Xilinx UltraScale™ MPSoC Architecture

The Right Engines for the Right Tasks

Ever smarter systems consume increasing amounts of communications and computing bandwidth. There are smarter phones, smarter networks, smarter data centers, smarter factories, smarter cars, and smarter energy systems, just to name a few. From the consumer to the enterprise, factories and infrastructure, there is more knowledge and vastly increased use of vision and location data, a greater need for guaranteed quality of service, increased security services, and other resources. “Big Data” (and small-data) applications need more and more analytics to automate control processing, provisioning, configuration, and overall system management.

Companies developing smarter systems that employ both hardware and software programmability will get to market faster and maximize end-product value while delivering additional benefits including adaptability, reuse, and rapid upgrade cycles. Xilinx has developed the UltraScale™ MPSoC (Multi-Processing System on Chip) architecture based on the defacto standard 28nm Zynq®-7000 All Programmable SoC and UltraScale All Programmable FPGA architectures to meet the expansive requirements for these new smarter systems including:

- Wireless Communications: Support for multiple spectral bands, smart antennas
- Wired Communications: Multiple wired communications standards, context-aware network services
- Data Centers: SDN (Software Defined Networks), data pre-processing, and analytics
- Smarter Vision: Evolving video-processing algorithms, object detection, and analytics
- Connected Control/M2M: Flexible/adaptable manufacturing, factory throughput, quality and safety

The UltraScale MPSoC architecture provides processor scalability from 32 to 64 bits with support for virtualization, the combination of soft and hard engines for real time control, and graphics/video processing, waveform and packet processing, next generation interconnect and memory, advanced power management, and technology enahancements that deliver multi-level security, safety and reliability.These new architectural elements are coupled with the Vivado® Design Suite and abstract design environments to greatly simplify programming and increase productivity.

This new architecture expands the numerous ASIC-class advantages inherent in the UltraScale All Programmable architecture—as first implemented and delivered by Xilinx using TSMC’s 20nm process technology, the world’s first commercial process technology to be based on double-patterned lithography.

The Zynq UltraScale MPSoC device family delivers unprecedented processing, I/O, and memory bandwidth in the form of an optimized mix of heterogeneous processing engines embedded in a next-generation, high-performance, on-chip interconnect with appropriate on-chip memory subsystems. The heterogeneous processing and programmable engines, which are optimized for different application tasks, enable the Zynq UltraScale MPSoC devices to deliver the extensive performance and efficiency required to address next-generation smarter systems while retaining backwards compatibility with the original Zynq-7000 All Programmable SoC family. The new UltraScale MPSoC architecture also incorporates multiple levels of security, increased safety, and advanced power management, which are critical requirements of next-generation smarter systems. The Xilinx Vivado® Design Suite and the UltraFast™ design methodology fully exploit the ASIC-class capabilities afforded by the UltraScale MPSoC architecture while supporting rapid system development.

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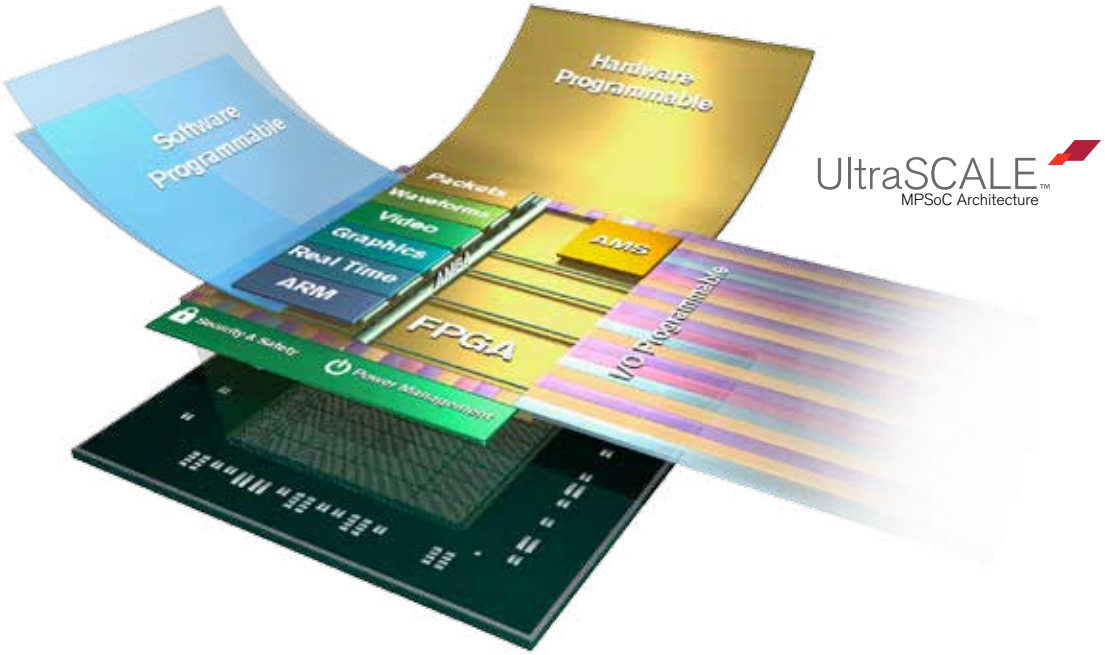

Figure 1: The Xilinx UltraScale MPSoC architecture delivers the right engines for the right tasks.

The Xilinx UltraScale MPSoC architecture, the Vivado Design Suite and additional design abstraction tools combine to break system-level processing bottlenecks through multiple technology breakthroughs.

Zynq UltraScale MPSoCs are a comprehensive device family of single-chip, All Programmable, heterogeneous multiprocessors that provide designers with software, hardware, interconnect, power, security, and I/O programmability. However, heterogeneous multiprocessing isn't just hard to say, it's hard to do—at least correctly. A design approach based on heterogeneous multiprocessing elements presents design teams with the following challenges:

- Meeting application performance requirements within a specified power envelope.
- Optimizing memory access and bandwidth for a heterogeneous-processing mix.
- Providing low-latency, coherent communications with adequate bandwidth among the myriad hard and soft processing engines.
- Finding a set of programming abstractions that permits fast system development and deployment while optimizing the mapping of system-level tasks to all available resources.
- Managing and optimizing system power consumption in all operational modes.
- Maintaining system integrity in the face of network-connected threats and harsh environments.

Failing to meet any of these challenges on time and within budget spells doom for a project.

Essential UltraScale MPSoC Architecture Elements

- The Right Engines for the Right Tasks
- Scalable to 64 bits
- Next-Generation Interconnect and Memory
- FPGA ASIC-class Scalability and Performance
- Multi-level Security, Safety, and Reliability
- Advanced Power Management
- 16nm FinFET Performance/Watt
- High-Level Design Abstractions
- Compatible with the Defacto Standard Zynq-7000 All Programmable SoC, Software, and Ecosystem

The Right Engines for the Right Tasks: A combination of new and next-generation processing and programmable engines, optimized for different application tasks.
The five processing bottlenecks (DSP, graphics, network processing, real-time processing, and general compute performance) cannot be overcome with one processing architecture. Many have tried to accommodate all of these processing tasks with a "one-size-fits-all" architecture and all who have tried this approach have failed. Heterogeneous multiprocessing using tuned programmable processing engines targeting specific task categories is the only certain path to success for complex system designs. Using the right engines for the right tasks provides performance, power, and cost benefits that smarter systems require to be efficient and effective in the market.

Scalable to 64 bits: Scalable from 32 to 64 bits with support for virtualization. Scalability includes not just the CPU but the on-chip interconnect, peripherals, processing engines, and the Terabyte address space.
Bigger and better CPUs and heterogeneous processing engines must be able to extend their enhanced processing power throughout the entire chip and beyond. This new UltraScale MPSoC architecture provides the required peripheral set, on-chip interconnect with massive bandwidth and an immense address space to overcome many critical gating factors for future system requirements and performance.

Next-Generation Interconnect and Memory: A next-generation coherent interconnect and memory subsystem that maximizes system performance, memory bandwidth, and task acceleration.
Software- and hardware-programmable engines that meet all processing requirements can still starve to death if their I/O and memory subsystems cannot meet processing throughput requirements. The UltraScale MPSoC architecture's advanced, scalable, and coherent interconnect—a further advancement of the UltraScale All Programmable logic architecture with its massive I/O and memory bandwidth capabilities—is optimized for the data-throughput needs of the UltraScale MPSoC architecture's on-chip heterogeneous processing engines. This capability is also shared across the processing and programmable logic domains to provide unmatched MPSoC performance and bandwidth.

FPGA ASIC-class Scalability and Performance: UltraScale ASIC-class logic fabric with ASIC-like features and optimizations for extreme real-time FPGA performance.
Software programmability is great for breaking through many processing bottlenecks, but not all of them. Sometimes, you just have to implement the processing solution in hardware to achieve the desired system-performance levels. The UltraScale MPSoC architecture's advanced ASIC-class capabilities builds on today's 20nm industry leading UltraScale programmable-logic architecture from Xilinx. Many of the architectural benefits are realized through the Vivado Design Suite's advanced development tools, which bring the full performance benefits of leading-edge programmable logic to bear on the most demanding processing challenges that can only be addressed by custom-designed hardware.

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Multi-level Security, Safety, and Reliability: Enhancements to anti-tamper features, trust and information assurance, operational safety and reliability that meet key industry standards.
With the explosive growth of the Internet of Things, machine-to-machine communications, and Smarter Connected Control, insecure communications and products are unthinkable. The UltraScale MPSoC architecture builds on Zynq-7000 All Programmable SoC leadership and includes multiple military-class security protocols to prevent any conceivable unauthorized access. The UltraScale MPSoC architecture also includes features that ensure that safety-critical applications can run reliably and provide the user and designer with the utmost confidence in their systems. This new architecture is designed to operate in the harsh environments that many Internet-connected machines inhabit and to meet the needs of smarter systems that work in these environments.

Advanced Power Management: Power-optimization and power-management features that enable fine-grained, system-level power reduction with software and run-time optimizations.
The UltraScale MPSoC architecture's diverse array of heterogeneous processing engines permits design teams to select the most efficient engine for any specific task, which enables task-based, system-level power optimization. The UltraScale MPSoC architecture's programmable-logic power management provides static- and dynamic-power management capability across a wide range of functional elements yielding significant additional power savings. The power management capability can be extended to the software-programmable processing elements by selecting the right engine to manage these tasks during operation of your systems.

16nm FinFET Performance/Watt: Full leverage of FinFET process technology resulting in a 60% improvement in performance/Watt across the UltraScale MPSoC's processing elements and logic fabric.
Design teams want and need to take advantage of the power, performance, and area benefits that FinFETs offer while still getting to market quickly and painlessly with strategically differentiated product designs. More than any other available alternative, Xilinx UltraScale MPSoCs architecture make this possible because they deliver all of the performance and power characteristics of FinFET technologies with none of the physical design risks, costs, or long development schedules required for a customer SoC or ASIC design. Leveraging the partnership built with de-facto standard 28nm Zynq-7000 All Programmable SoCs and industry-leading 20nm UltraScale FPGAs, Zynq UltraScale MPSoCs built on TSMC's 16nm FinFET process give designers up to 60% improvement in performance/Watt over 28nm process technology.

High-Level Design Abstractions: Tailored, system-level design environments based on C, C++, and OpenCL with design flows based on IP subsystem reuse
The Xilinx UltraScale MPSoC architecture supports multiple abstraction layers to push far beyond traditional RTL design methodologies. The Vivado Design Suite and additional design abstractions including C, C++, SystemC, OpenCL, OpenCV, MATLAB, and LabView create the industry's most comprehensive, mixed-abstraction, system-design environment, which automates all aspects of system development. This environment provides productivity benefits, fast development of software compatible hardware accelerators, and permits fast algorithm deployment into devices based on the UltraScale MPSoC architecture while allowing design teams to leverage any set of design abstractions that best fit the target application.

Compatible with the Defacto Standard Zynq-7000 SoC, Software, and Ecosystem: Software migration capability to allow upgrade of applications, OS, middleware, IP, tools, and a broad ecosystem drawn from today's defacto standard, the Xilinx Zynq-7000 All Programmable SoC.
The Zynq-7000 All Programmable SoC consists of more than Generation Ahead silicon. It has become the industry's defacto standard for All Programmable SoCs because it is a comprehensive platform with an immense ecosystem of software solutions, tools, IPs, boards—including the industry-leading Vivado HLS high-level synthesis tool that greatly accelerates design productivity by permitting design teams to create hardware from descriptions written in C, C++, or OpenCL. Other popular, leading-edge design tools such as MATLAB and Simulink from The MathWorks and the graphical LabView design environment from National Instruments have already been adapted for the Zynq-7000 platform to enable multidimensional, high-level system design that greatly improves designer productivity.

All major operating systems are available for use with the Zynq-7000 All Programmable SoCs. In addition, system design teams

can choose from many SOMs (System on Modules), as well as a broad application-specific ecosystem of middleware and programmable IP to meet the diverse needs across the many applications where Zynq SoCs are currently used. This broad ecosystem is already embracing the Xilinx UltraScale MPSoC architectural extensions.

Put all of these elements together and this is the picture that emerges:

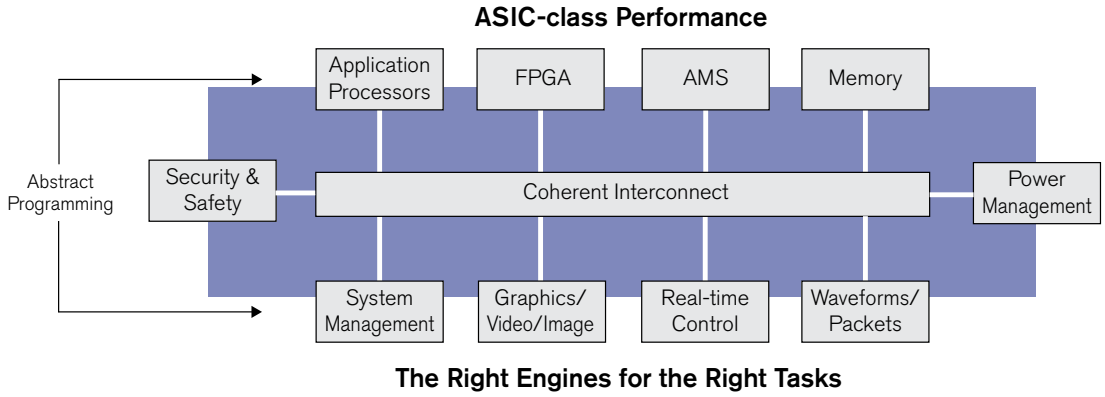

Figure 2: The Xilinx UltraScale MPSoC architecture delivers the right engines for the right tasks.

Only Xilinx has the track record of innovation, execution, quality, access to the complete mix of All Programmable and UltraScale architectures and other essential technologies needed to create ASIC-class devices like the Zynq UltraScale MPSoC family. These essential technologies include:

- The proven UltraScale All Programmable architecture built upon the most advanced TSMC 16nm FinFET process technology
- The award-winning Zynq SoC architecture, which has become the industry's de-facto standard—now expanded into the heterogeneous UltraScale MPSoC architecture
- Second-generation SSI (stacked silicon interconnect) 3D IC technology, which enables "More than Moore" system scaling with more than double the capacity and a 50% bandwidth advantage versus competitive programmable-logic products
- The industry's only ASIC-class, SoC-strength development environment based on the Vivado Design Suite with MPSoC extensions for C, C++, and OpenCL specifications and many additional design abstractions

For more information about Generation Ahead system design based on Xilinx Zynq UltraScale MPSoCs, contact your local Xilinx sales office.

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