DesignCon 2015

Co-Design for 1TB System Utilizing 28Gbps Transceivers in 20nm Technology

Hong Shi, Xilinx
[hongs@xilinx.com]

Sarajuddin Niazi, Xilinx
sarajud@xilinx.com

Romi Mayder, Xilinx
romim@xilinx.com

Ravindra Gali, Xilinx
ravindr@xilinx.com

Abstract

The traditional boundary of interconnect design between silicon, package and board is becoming increasingly blurred as we move to higher data rates with each technology node. It is now commonly recognized in the industry that power consumption is the biggest bottleneck when implementing silicon equalization to address 1-TB system markets. New package architecture in conjunction with on-die compensation can offer additional margin to system jitter budget and mitigates extensive equalization requirements. This paper describes co-design methodology on a test vehicle during the development of Xilinx's 20nm FPGA device family with embedded transceivers capable of operating at 30.5 Gbps.

Author(s) Biography

Hong Shi is Director of Package Design at Xilinx, driving architecture and product development along with design methodology for FPGA packaging platforms supporting ultrahigh speed signaling, IO, AMS, fabric and processors. Previously, he has worked at Altera, Agilent, Hewlett-Packard. Hong Shi holds a Ph.D. in Electrical Engineering from the CREOL School of Optics, University of Central Florida; MSc. in Physics from DePaul University, Chicago; MSEE, BSEE from Xi'an JiaoTong University, China. He holds 30 patents and has authored over 60 technical articles and one book chapter in refereed journals and conference proceedings. In recent events, he is chair of the high performance high density 3D/2.5D package panel at DesignCon 2014. He is the keynote speaker in SEMICON China/CSTIC 2014 Package and Assembly Symposium.

Sarajuddin Niazi is currently a Staff Signal/Power Integrity Engineer at Xilinx, Inc. At Xilinx Mr. Niazi responsible for developing Package solution for high speed Serdes.

Mr. Niazi joined Xilinx three years ago prior to joining Xilinx, Mr. Niazi worked at Startup Company specializing in low loss high-speed interconnects design. Mr. Niazi received his Bachelor of Science degree in Electrical Engineering at the University of California at Davis. Mr. Niazi has a patent application in the field of Signal integrity.

Romi Mayder is currently a Director of Applications Engineering and Technical Marketing at Xilinx, Inc. Prior to joining Xilinx, Mr. Mayder worked as a consultant specializing in silicon die level signal and power integrity. He also consulted in the field of design and fabrication of advanced package technologies, including stacked silicon interconnect. Mr. Mayder has been employed by two companies in the Test and Measurement industry, Agilent Technologies and Anritsu (Wiltron) Company, where he specialized in microwave and millimeter wave microelectronic circuit design and fabrication. Additionally, Mr. Mayder has over 10 years of experience in semiconductor process technologies including photolithography, ion implantation, plasma enhanced chemical vapor deposition, dielectric sputtering, and chemical mechanical polishing of silicon wafers. Mr. Mayder received his Bachelor of Science degree in Electrical Engineering and Computer Science from the University of California at Berkeley in 1992. Mr. Mayder has published 25 patent applications in the fields of signal and power integrity as well as semiconductor process technologies.

Ravindra Gali is currently a Staff Product Applications Engineer focusing on Signal/Power Integrity at Xilinx, Inc. Prior to joining Xilinx, Mr. Gali worked in various roles as a SI/PI Design/Application Engineer at Altera, Intel & Dell focusing on PCB/Package Signal and Power Delivery issues. Mr. Gali has over 10 years of industry experience along with an MSEE and MBA degree from New Mexico State University and San Jose State University respectively. Mr. Gali has a patent application in the field of signal and power integrity as well.

Introduction

The demand to 400G/1TB data path requires high speed transceivers operating at 28Gbps line rate today and 56Gbps in the next three years for low power and economical system implementation (Figure 1). As carrier frequency and harmonics going into millimeter wave domain, semiconductor IC package industry enters an unfamiliar world where many challenges become fundamental to the legacy technology and design practices. In the meantime, photonics interconnect gains increasing momentum due to its reach and power saving, making many question whether copper based will give way to optical ones soon.

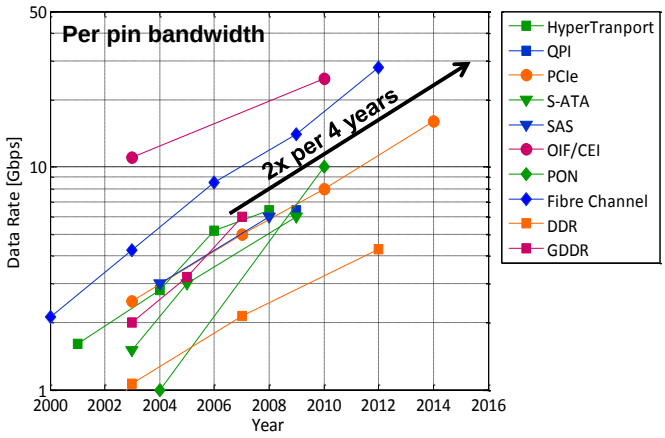


Figure 1. SerDes rate doubles every four years or equivalently every two nodes. (Source: ISSCC wireline subcommittee [1])

In copper based IC packages, interconnect impairments can be categorized into three areas: inter-symbol-interference (ISI); crosstalk (XT); power supply induced jitter (PSIJ). The net effect is bit error associated with reduced bandwidth and increasing coupling noise from channels and powers. Up to 28Gbps, silicon equalization has adequately compensated the data link against various impairments at the expense of ever complex circuitry and power consumption. High power consumption from equalization circuits, particularly DFE has made active compensation approach to diminishing return.

The power bottleneck becomes more severe to long reach protocols. Figure 2 is collection of industry 10-28Gbps implementations by ISSCC on various reaches and associated power efficiency. The power consumption is roughly estimated increasing at rate of 10X per 20dB loss. The 35-dB marks the highest channel loss that most silicon chips today can compensate across industry. As 56Gbps components are emerging, silicon equalization becomes overwhelmingly challenged in circuit complexity and power consumption. The traditional world of IC packages needs to innovate to minimize the interconnect impairments.

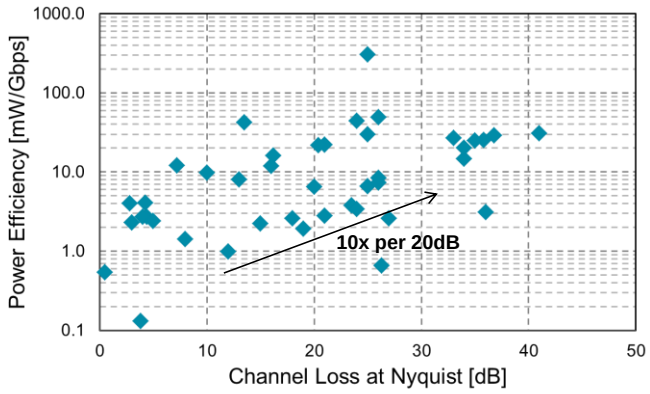


Figure 2. Power efficiency as function of channel loss or link reach (Source: ISSCC wireline subcommittee [1])

This Paper

We describes a unique co-design methodology with new package architecture in conjunction with on-die compensation to provide very low jitter interconnect for 1-TB applications. This methodology yields additional margin to system jitter budget and mitigates equalization requirements.

The paper is divided into four main sections. The first section talks about the interconnect impairments and physical root causes. The second section describes co-design strategy to minimize the impairments. It includes a new design methodology, namely "skip-layer" stackup beneficial to not only serdes channels but also to analog power distribution networks. The third section extends analysis to system level and compares the effects of equalization to traditional baseline and "skip-layer" package designs respectively. The last section is devoted to forward looking 56Gbps package design. A recent disruptive advancement is stacked silicon integration technology (SSIT) and its role in 400G/1TB system solutions is also reviewed.

Package Interconnect Impairments

To best describe all the key impairment factors, an interconnect transfer function concept is introduced, where magnitude is a function of return loss, material loss, crosstalk and radiation, and phase relates to dispersion.

Insertion Loss and ISI

In IC packages, losses are from both metal trace and dielectric. Dielectric loss is proportional to product of frequency and loss tangent [2]. It means that a 56Gbps package substrate needs to seek dielectric materials possessing one half of loss tangent of 28Gbps package in order to meet the same loss specs. Most of 28Gbps packages today use 0.007 DF materials across industry. Thus, 0.0035 or less will be the technology target for 56Gbps packages.

Metal loss has different characteristics depending on profile and frequency range. It is dominated by skin depth in organic substrate (metal trace thickness is of ~15um) and by resistance in silicon interposer (metal trace thickness is about sub-um). Figure 3 describes skin depth of copper foil as function of Nyquist frequency. It states that 20Gbps data transmits at ~0.7um (r.m.s.) deep into metal surface, 28Gbps at ~0.6um. The 56Gbps signal is at merely 0.4um thin region of metal surface

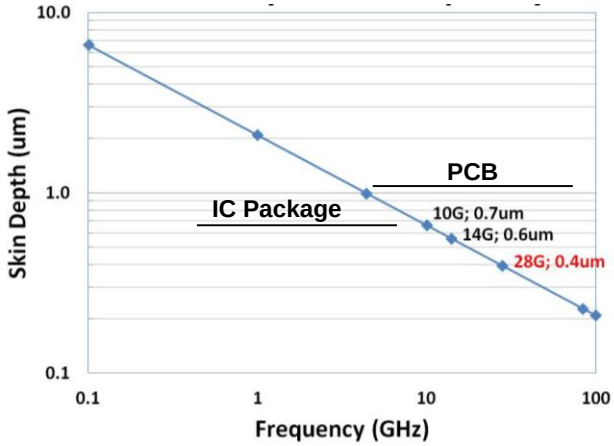


Figure 3. Skin depth as function of Nyquist frequency

Depending on copper surface treatment, the Ra (arithmetic average roughness) varies from ~1um to 0.6um in most packages. A few analytical studies have provided metal roughness effect but none compares to dielectric loss at extremely high frequency [3]. Our modeling study shows surface roughness is more dominant than dielectric loss at 28Gbps and above. Thus, it is critical to realize low Ra for 56Gbps packages, which is a new challenge to substrate industry.

Figure 4 depicts elements of Xilinx's Stacked Silicon Interconnect Technology (SSIT) [3]

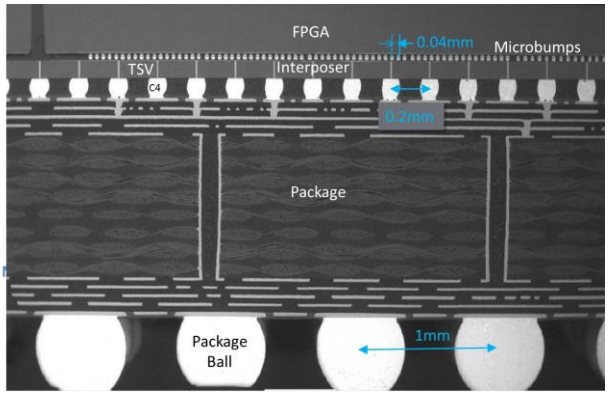


Figure 4. Stacked Silicon Interconnect Technology

Because of finite silicon conductivity, through silicon vias (TSV) forms frequency varying capacitor. At ultrahigh frequency, bulk silicon behavior dominates the loss curve. Frequency dependent TSV loss needs to be included in high speed package design. Figure 5 shows nearly 0.5dB loss is introduced by TSV. To offset the SSIT loss, the organic substrate needs to be designed with extra margin.

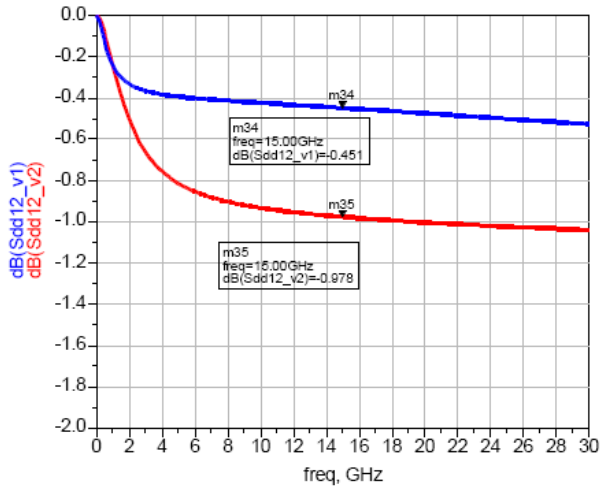


Figure 5. Insertion loss comparison between SSIT (TSV) package and conventional monolithic die package (Source: N. Kim, et al. DesignCon 2011 [6])

Reflection from impedance discontinuity often poses itself as the greatest loss term in many designs. The root cause comes from fundamental constrain of today's package technology and certainly sub-optimal design practices. In BT material core packages, the core via is formed by mechanical drill followed by copper plating, aka. plated through hole (PTH). As die bump pitch is ever decreasing to below 200um range to accommodate silicon density over the past technology nodes, PTHs remain at ~300um. Large pad and pitch introduce parasitic capacitance and inductance significant to high speed bandwidth loss. Figure 6 illustrates why large via pad and pitch is not preferred.

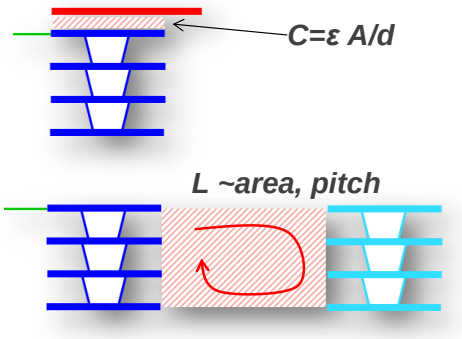


Figure 6. Signal transverse in vertical direction inside package

Crosstalk

In a die-package-PCB interconnect environment, crosstalk is mainly caused by inductive coupling. Signal transitions through the PTH via field are the most common places where limited spacing between the aggressor vias and a victim via does not provide adequate isolation to inductive coupling. Figure 7 shows a portion of the typical transceiver package BGA pin map. shown below, there is shielding between adjacent pairs using mixed power-ground pins. However, each RX pair sees two TX pairs diagonally. The PCB PTH vias in the breakout region follow the BGA pattern and accumulate inductive coupling linearly with the depth of the PCB via.

Figure 8 illustrates a close-up of BGA-PCB breakout junction. The ground plane underneath the Tx & Rx trace routing is not shown. Figure 9 captures the power sum near-end-cross-talk between diagonal transmitter and receiver. This level of inductive coupling is often acceptable for 10Gbps signals, where the ratio of insertion loss to coupling is large enough for silicon equalization to restore eye margin loss. However, the coupling becomes the most detrimental effect at 28Gbps and beyond.

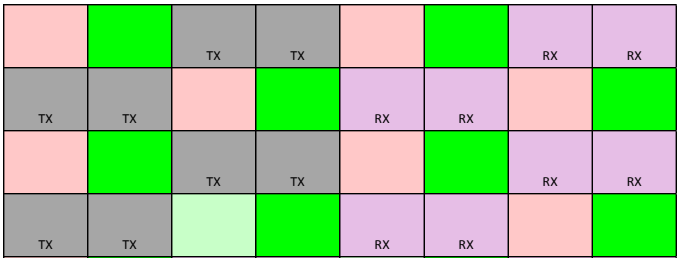


Figure 7. Pin map for one quad of serdes lanes. Green is ground and orange is power

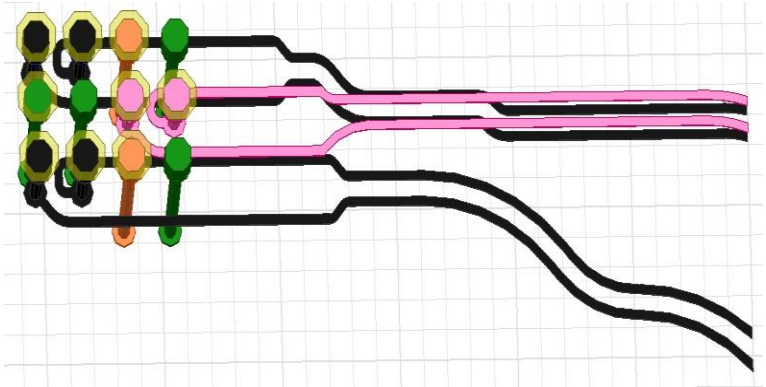


Figure 8. BGA-PCB Breakout Junction (TX/RX routed on different layers)

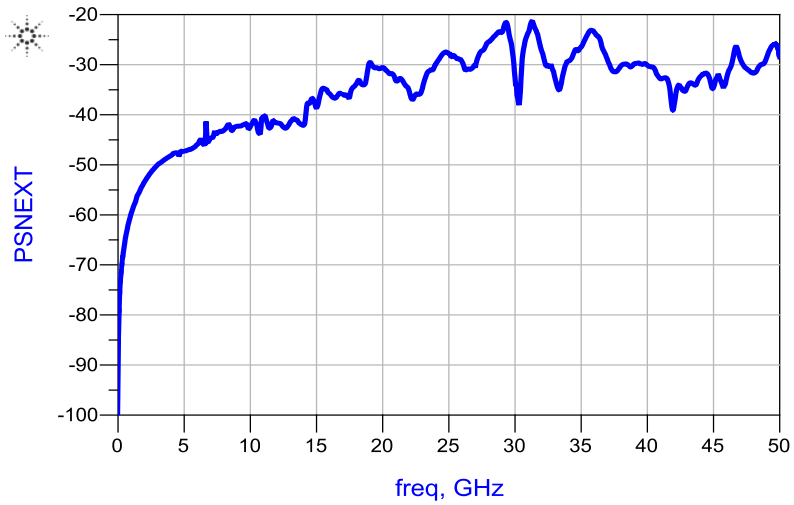


Figure 9. Cross coupling for typical BGA pin map (power sum from BGA side)

Co-Design Strategy and Implementation

In this section, we will introduce three co-design schemes to mitigate interconnect impairments. First, the physical and circuit features are implemented, and then modeling comparison is made to demonstrate the advancement results.

"Skip Layer" Stripline

The metal loss can be reduced by low Ra surface. Alternatively, wider metal trace width can effectively reduce the surface resistance and reduce the signal current density in rough Ra region. To maintain the characteristic impedance, wider width would require higher dielectric thickness. As a result, the skip layer concept is formed by using two nominal dielectric layers to replace one layer at top and bottom of stripline. Figure 10 shows the stackup cross section of a conventional 93Ohm stripline and skip-later 93Ohm transmission line.

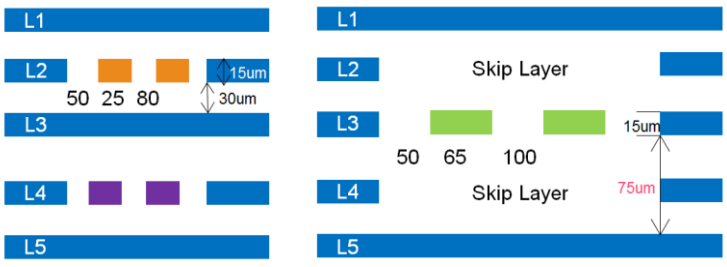


Figure 10. Stackup and dimension of conventional and skip layer stripline (50um, 65um, 100um correspond to ground-signal separation, trace width and signal separation)

It can be observed that both DP and DM signals are broadened from 25um to 65um. Effective dielectric thickness is 75um as compared to nominal 30um. Accordingly, other dimensions are adjusted to keep the same characteristic impedance as that in single layer stripline. Figure 11 show improvement of ~0.67dB at 16.5GHz.

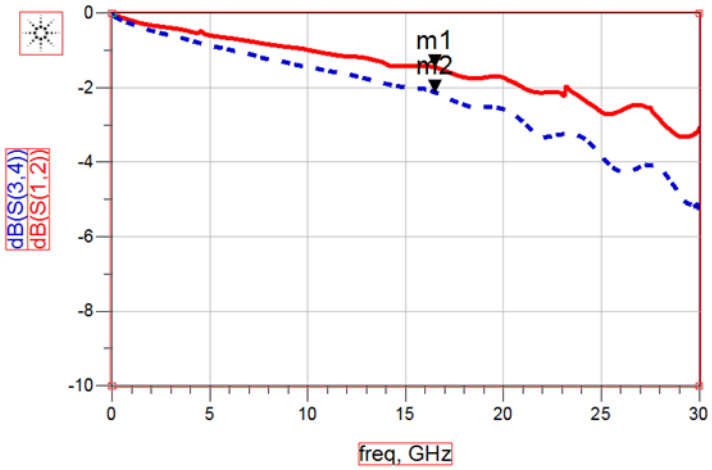


Figure 11. Insertion loss of skip layer (red solid) as compared to conventional (blue dash)

The 0.67dB gain to insertion loss is equivalent to approximately lowering surface roughness Ra by 3X. In today's packaging industry, the low Ra treatment faces various challenges from quality, yield, manufacturing process, to eventually cost. The skip-layer stripline provides a design choice to mitigate loss ahead of technology breakthrough. The additional layers incurred can be leveraged for analog power plane. For example, the L2 and L4 layers are best used to form low spreading inductance power planes with ground layers. As a result, the PSIJ control can take significant advantage from skip layer package.

On-Die Compensation

At interface of die and package, various structures are capacitive discontinuities causing signal reflection and bandwidth shrink. The capacitive structures include die pin capacitance, C4 bumps, and microvia pads on top layers of package. In SSIT packages, TSV also contribute towards some extra capacitance. In order to minimize the discontinuity, an on-die inductor is implemented in the last stage of the TX driver. This localized inductor provides impedance offset to compensate the capacitive droop. It should be pointed out that the added inductor forms a second order filter to achieve max flatness response only in certain frequency range. Specific design parameters must be chosen for target bandwidth.

Figure 12 shows improvement to return loss and insertion loss. It can be seen the improved response flatness is from DC to ~17GHz. At frequencies greater, the response slope is at ~40dB/decade and rolls off rapidly. It is important to notice that combined die and package has made the overall insertion loss lower than package only (Figure 11), which states the needs for on-die compensation.

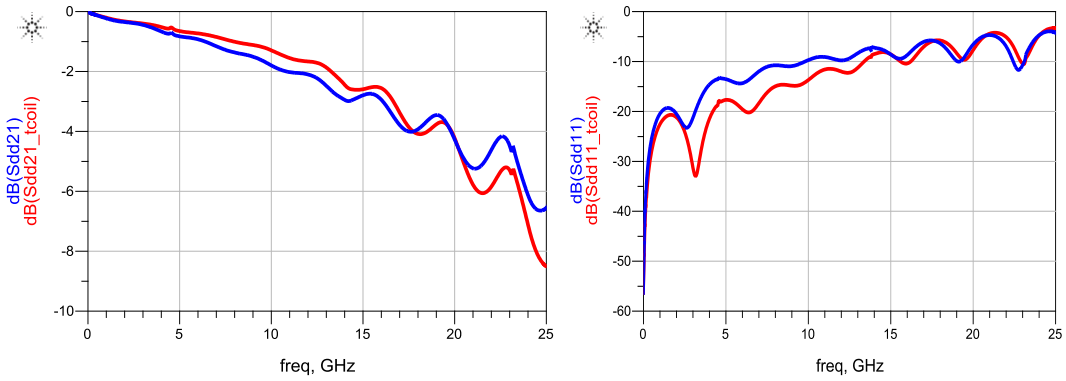


Figure 12. Effect of on-die inductor to combined die-package channel insertion loss and return loss compensation. Red is with compensation inductor.

Pinout and PCB Escape Enhancement

To increase the margin between insertion loss and crosstalk we insert a wall of ground pins between TX/RX. As such the TX and RX pairs are completely shielded by solid ground pins in all directions. Figure 13 shows cross coupling is significantly reduced between diagonal TX and RX. The average reduction in coupling after cross talk optimizationis approximately 10dB which is more than sufficient to enable 28Gbps signaling across long reach channel.

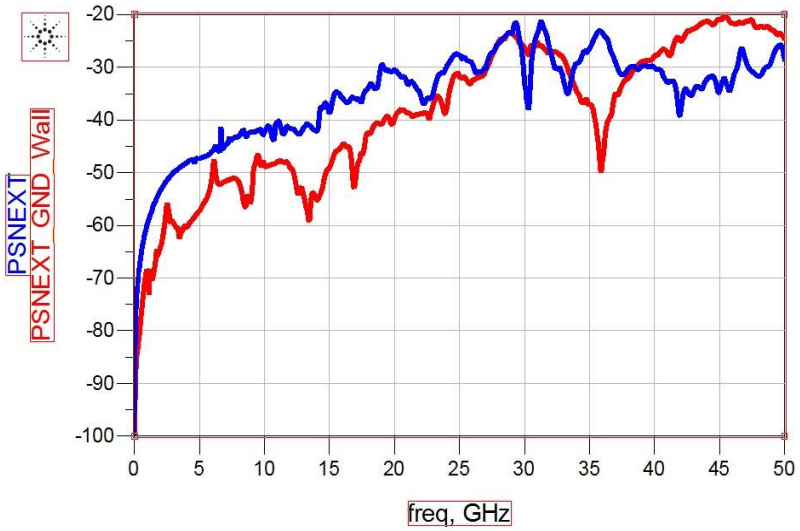


Figure 13. Effect of ground pin wall on cross coupling. Blue is result from typical pinmap like the one shown in Figure 7. Red is result from adding solid ground wall separating TX from RX in all directions

Circuit and System Level Analysis

Time domain simulations were performed on a baseline package and the optimized test vehicle package to study the performance differences. The simulation setup consists of an ideal driver running a PRBS31 pattern at 28Gbps through a TX and RX package channel model cascaded together. A differential (pk-pk) voltage of 0.916V with no pre-emphasis is applied at the driver with a rise time of 15ps. Both the driver and receiver are assumed to have a 100Ohm load with CTLE/DFE disabled at the receiver. The eye opening is observed at the receiver for both the scenarios. To minimize the run time of the simulations, the simulation run was limited to 1million bits in a bit-by-bit mode in ADS.

Figure 14 shows eye diagram comparison to two package designs. As one can see from the simulation results, the jitter performance of the optimal design package is significantly better than the base line package. The jitter (pk-pk) number for baseline package is 5.71ps whereas the jitter for the test vehicle package is 1.8ps, an improvement of roughly 68%.

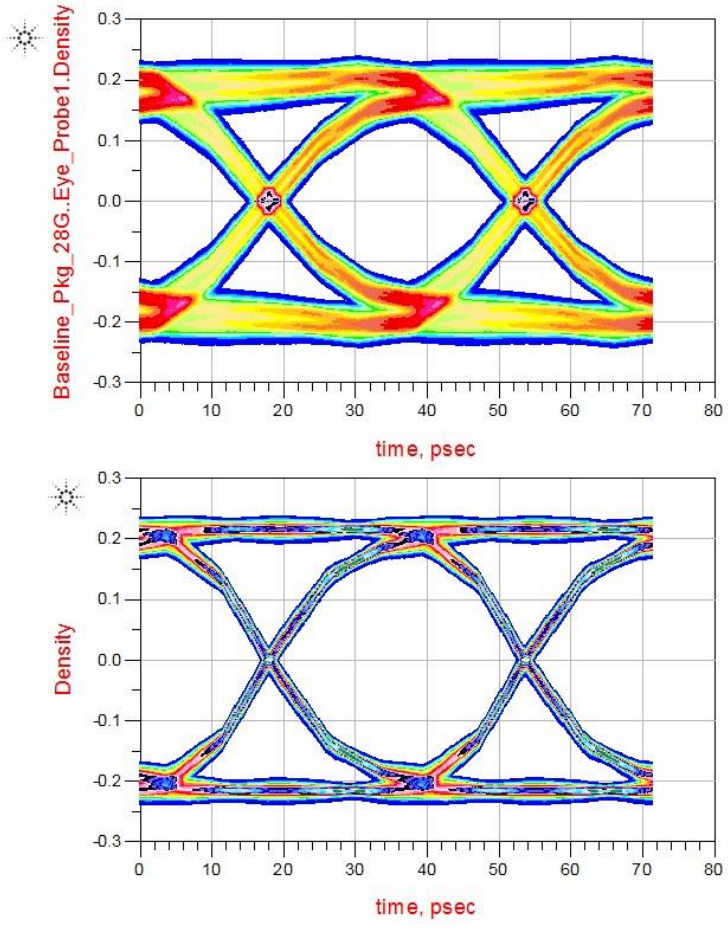


Figure 14. TX and RX package only simulations. Top eye diagram: baseline package. Bottom eye diagram: optimal design.

Next simulations were performed by introducing a very short reach (VSR) channel and observing the package performance between the two different packages as shown in Figure 15. The VSR channel is a 3.5” 100ohm differential pair PCB trace model with an insertion loss of roughly 3dB at Nyquist frequency of 14GHz. For this simulation, the driver assumes a 3dB pre-emphasis for both the scenarios. No CTLE/DFE was enabled at the receive side for both the cases.

As you can clearly see, the optimized test vehicle package with skip-layer, low loss dielectric and PTH via optimization clearly shines compared to the base line package without any of these enhancements. There is a roughly 20% improvement in the horizontal eye opening with a roughly 30% vertical eye opening between the two packages.

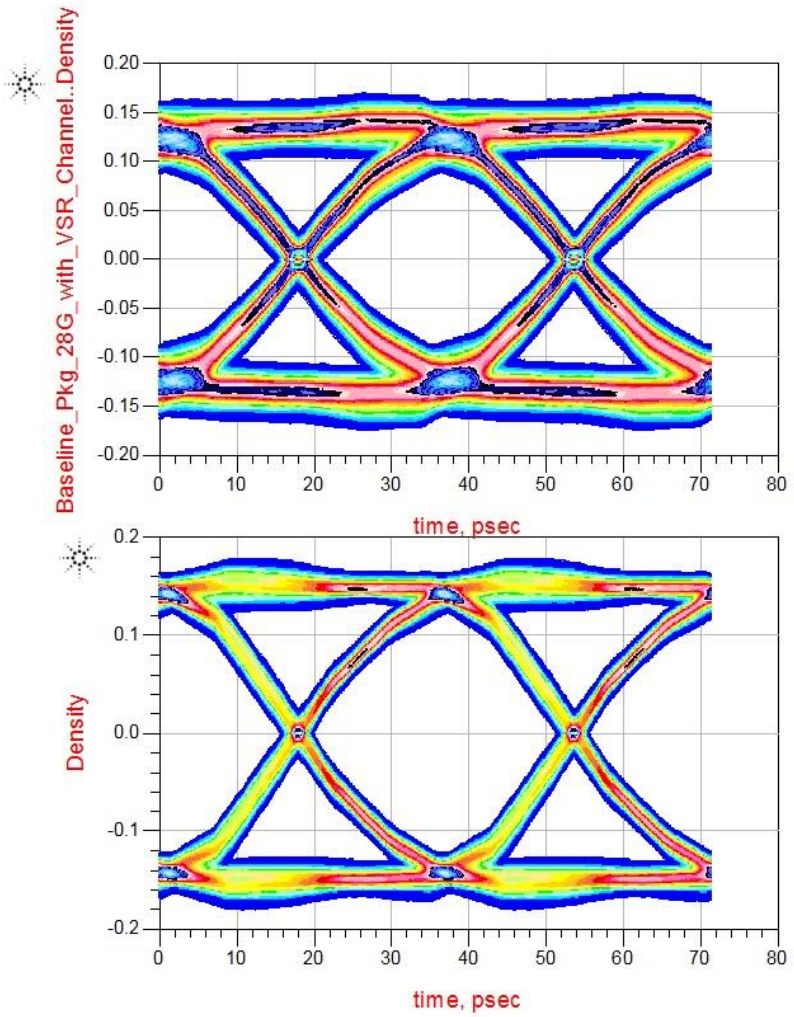


Figure 15. TX and RX package in a 28Gbps VSR system. Top eye diagram: baseline package. Bottom eye diagram: optical design

Additional simulations were performed on the baseline package to determine if extra pre-emphasis boost on the driver will result in similar jitter (pk-pk) performance as seen on the test vehicle package. An extra 2dB of boost is needed on the baseline package and with the VSR channel at 28Gbps to see an improvement in jitter performance. However, the resultant improvement in jitter performance still lags behind the jitter performance seen on the test vehicle package.

As a final comparison, simulations were performed on the same VSR channel at 56Gbps, as shown in Figure 16. The total insertion loss for the simulation setup with the optimized test vehicle package was roughly 13dB compared to 20dB for the base line package configuration. For this simulation the rise time from the ideal driver with a PRBS31 data pattern is assumed as 8ps with a 6.5dB pre-emphasis for both the configurations. The simulation assumes that the CTLE/DFE is disabled to study the effect of package optimization.

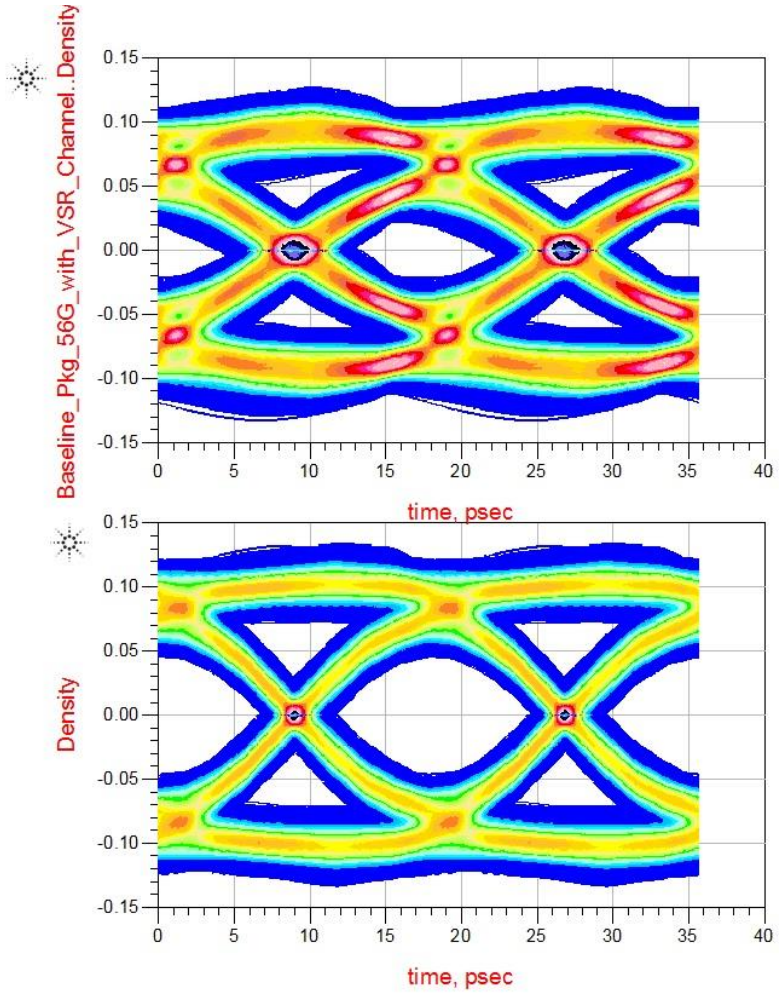


Figure 16. TX and RX package in a 56Gbps VSR system. Top eye diagram: baseline package. Bottom eye diagram: optical design

The simulation clearly shows that the optimized test vehicle package has a 50% improvement from a jitter (pk-pk) perspective along with a roughly 62% improvement on the vertical eye height. Coming to the 56Gbps scenario, an additional boost of 3.5 dB compared to test vehicle package still pales in comparison to the horizontal and vertical eye opening seen on the test vehicle package. Additional simulations with different pre-emphasis settings didn't yield any subsequent improvements as well.

56Gbps Package Forward-Looking

In the last section, most recent technology advancements are reviewed in area of organic substrate and stacked silicon integration platform for 56Gbps. In a recent study, various substrate technologies are compared and shown in Figure 17 for excessive parasitic capacitance and inductance. The maximum capacitance is derived by assuming via pad entirely covering adjacent metal layer. The minimum inductance is derived from inductance at the smallest via pitch that manufacturing process allows. It can be seen that option 2 and 5 are most desired combination regarding via pad and pitch.

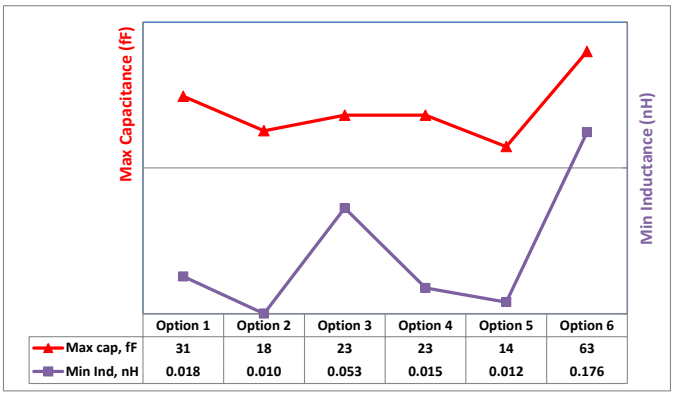
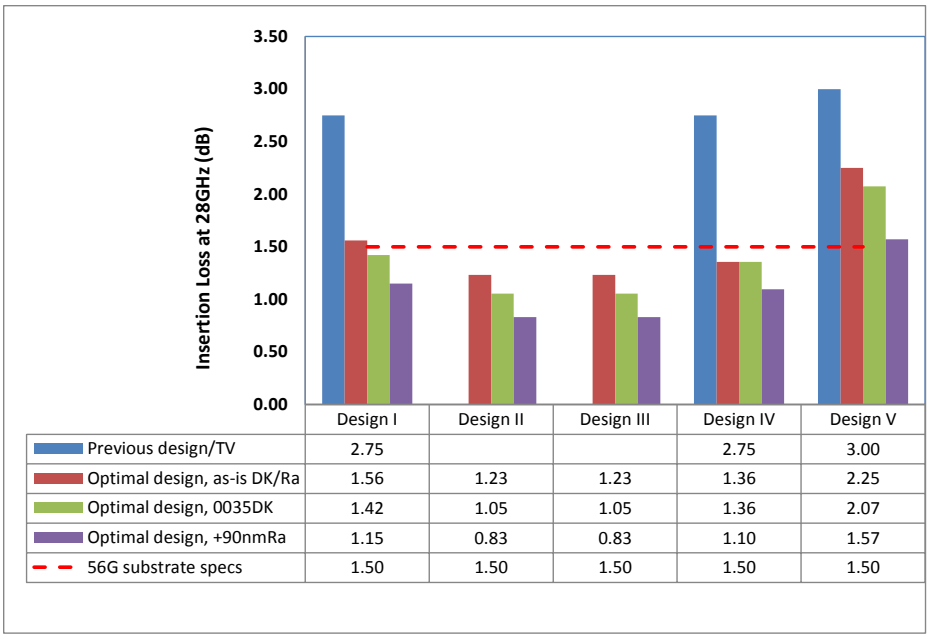


Figure 17. Parasitic capacitance and inductance as function of pad diameter and pitch

Furthermore, analytical study reveals potential performance differences from different package designs made by various substrate options. The takeaway is that small pad size and pitch is crucial for insertion loss reduction. Material quality can provide further margin.



	Design I	Design II	Design III	Design IV	Design V
Previous design/TV	2.75			2.75	3.00
Optimal design, as-is DK/Ra	1.56	1.23	1.23	1.36	2.25
Optimal design, 0035DK	1.42	1.05	1.05	1.36	2.07
Optimal design, +90nmRa	1.15	0.83	0.83	1.10	1.57
56G substrate specs	1.50	1.50	1.50	1.50	1.50

Figure 18. Channel insertion loss at 28GHz on five designs utilizing different substrate

[7]. Figure 19 illustrates Xilinx's Stack Silicon Less Interconnect (SLIT) technology and its differentiation to conventional silicon interposer [7]. The noteworthy difference is the TSV less 3D interconnect. By eliminating TSV, the intrinsic capacitor and associated high frequency loss is eliminated. It solves the most noteworthy issues since the beginning of utilizing silicon interposer as integration platform for high speed transceivers.

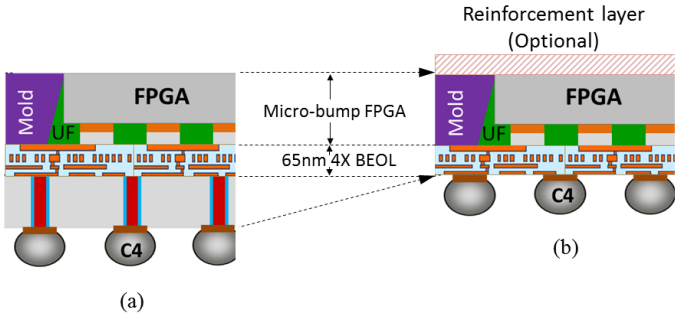


Figure 18. Comparison of the structures of Stack Silicon Interconnect (SSI) of (a) using TSV interposer and (b) new interconnect scheme (Source: W. Kwon et al, IMAPS 2014 [7])

Summary

Package design plays a pivotal role in a high speed system in which silicon equalization is limited by power consumption and circuit complexity. Skip-layer, on-die inductor, and solid ground wall separating TX and RX pins are a few package design innovations enabling the high speed serdes devices to achieve 28Gbps lane rate in 1-Tb systems. Further reduction to substrate feature size and new low loss material are studied for 56Gbps packages. The recent breakthrough SLIT interposer technology is showing promise in removing the TSV loss entirely.