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Comprehensive Full-Chip Methodology to Verify EM and Dynamic Voltage Drop on High Performance FPGA Designs in the 20nm technology

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Abstract

The convergence of advanced process technology, increasing levels of integration and higher operating frequencies pose considerable challenge to FPGA designers whose circuits are required to function in variety of conditions. Full-custom and mixed signal circuit designers ensure that their circuits will function by simulating for various operating conditions (PVT, input stimuli, etc). One key aspect for the reliable operation of these complex circuits is the quality of the voltage supply they receive. However, it is becoming increasingly apparent that traditional and existing methods of considering power supply variation and noise is grossly inadequate and do not consider the multiple factors that contribute to power and ground supply noise. Also existing methods do not provide sufficient capabilities to predict the impact of the fluctuation in the power and ground supplies on various key circuit parameters like noise margin, clock jitter, and delays. Additionally, in traditional IC design methodologies, the custom IPs are typically designed and verified independently of the environment they operate in. However, the impact of integrating digital and mixed-signal IP blocks in FPGA and ASICs is considerable and is manifested in both directions – from the IP to the chip and from the chip to the IP. The critical area of power noise analysis and reliability verification targeting analog and mixed signal circuits, both by themselves and in context of the chips they operate in, have not been adequately addressed by existing solutions. There is a clear and present need for an integrated analysis, verification and optimization methodology.

Author(s) Biographies

Sujeeth Udipi graduated from PSG College Of Technology, India with a Bachelor's degree in 1994 and from Arizona State University with a Master's degree in 1997. Since then, he has worked on circuit design and CAD methodology at Sun Microsystems (1997 - 2010) and currently works on EM-IR methodology and tool deployment at Xilinx Corp.

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Introduction

In this paper we present a comprehensive methodology for power-noise-reliability sign-off for 20nm FPGA designs, taking various aspects of analysis needs (coverage, accuracy, co-design etc.) into account. This paper talks about a comprehensive co-simulation framework for analog, mixed-signal, and custom circuit designers to sign-off "full-chip" FPGA designs by taking into account the impact of chip, package and system as shown in Figure-1.

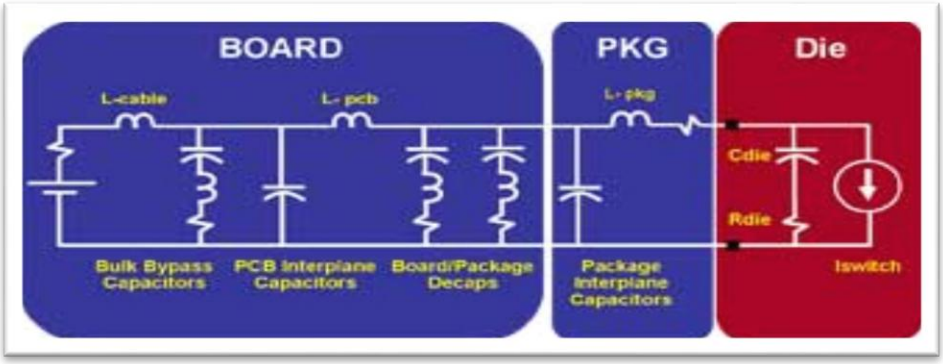

Figure-1: Chip-Package-System Power-Delivery-Network

This paper will summarize the key requirements for the 20nm FPGA design verification and how this can be achieved using practical examples of the following:

- Power-noise-reliability verification flow to independently validate the blocks at a transistor level and study the effectiveness of various design aspects.
- Electro-migration signoff using vectored and vector-less methodologies.
- Generate accurate models that can be used in the top level simulations providing transistor level detail without compromising run-time and capacity.
- Power-noise analysis of the FPGA integrating the various IP models to predict both global and local power noise through the power grid, package and board.

Failure of conventional approaches

Power noise and its impact is a well-known and long studied phenomenon. However, solutions and methodologies have not kept up with the challenges associated with the needs and requirements for comprehensive power noise analysis for today's designs. Traditionally, circuit designers have used static voltage drop analysis to identify and prevent power supply related issues. Static voltage drop analysis provides the ability to quickly check the general weaknesses in the power and ground network by using average current consumption of every device and solving Ohms law. However, static IR analysis does not consider the impact of capacitance and inductance of the power ground network on voltage drop, but is rather a DC solution of the voltage drop based on average currents. Static analysis can be used to find gross weaknesses during early design phase; however it does not accurately describe the true transient nature of the power and ground noise. Neither can it be used to understand the coupling of noise through the substrate network, nor can it be used to understand the impact of switching of one block on another. *Figure-2* clearly illustrates the difference between static / DC and dynamic / transient analysis. For the former a constant current is used to mimic current draw while for the latter the true transient switching current (along with leakage) is used to reflect the operation of the chip.

To capture the transient nature of power and ground noise on circuits, the design industry has historically relied on spice or fast-spice approaches for analysis. Fast-spice simulators have some inherent shortcomings when they are used to analyze or validate power-ground noise impact on circuits.

Capacity: Design complexities and design sizes have far outpaced the performance improvements provided by fast-spice simulators. Even though fast-spice simulators utilize methods such as model reduction, model reuse, and current mode modeling they have been unable to keep up with the growing pace of a power grid's RLC network complexity. Typically, adding a power ground RLC network to a transistor level net-list will cause fast-spice simulator to choke due to the large channel connected regions seen by the simulator. These simulators have not been able to provide a viable solution for power-ground analysis in a reasonable amount of time.

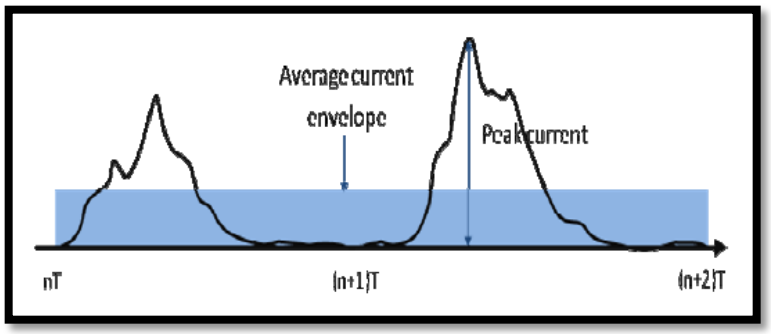

Figure-2: Static Average vs. Dynamic Peak Envelope

Usability: Fast-spice simulators do not follow a single kernel approach for power-ground network analysis. The parasitic net-list is typically extracted using a third party extraction engine and simulated by combining the pre-layout net-list with the post-layout extraction results. Moreover, the ability to clearly identify IR and EM bottlenecks in power-ground networks is far from easy using this approach.

Co-simulation: Fast-spice simulators cannot integrate into a full-chip analysis framework for power and ground noise. For the bottom-up design verification methodology, IP designers should be able to analyze the IPs independently and generate models that can be integrated into a full-chip analysis framework. Fast-spice simulators have not been able to keep up with the complexity and size of FPGA designs for any type of hierarchical analysis.

Interactive Fix and Verification: During IP level EM/IR validation, it is necessary to model incremental design changes to the power grid, bypass-cap placement and decoupling-cap placement. The turn-around cycle for such types of changes and analysis usually involves making a layout change followed by extraction of the layout and then simulation of the design. Such large validation cycles are no longer a luxury in today's compressed tape-out schedules.

The lack of high capacity, full-chip level substrate noise analysis tools have driven designers to employ several techniques to ensure that they have sufficient protection and isolation for their sensitive circuits from other logic on the chip. They use simplified Spice net-lists to predict such scenarios or use silicon measurement data from one version of a chip to define the design methodology for the next generation of the chip. However, both of these techniques are rife with issues and limitations. The former is limited in scope and cannot comprehend the full-chip scale and the nature of substrate noise injection and propagation. The latter approach relies on the belief that past design techniques and measurements will be good indicators for future designs.

Methodology

The methodology provides the ability to perform transistor level static and dynamic power noise analysis both at the IP and at the full-chip level. These analyses provide coverage for timing and functionality verification from impact of power and ground bounce and reliability verification from the flow of current in the power and ground lines. Additionally, it provides support to perform signal line electro-migration analysis. In this section, the data requirements, modeling flow and usage of the flow both for block validation and full-chip level analyses will be discussed. The following table in *Figure-3* defines how the overall sign-off is achieved.

Flow	Must Check	Coverage	What Is Checked?
Static	IR / AVG-EM	100%	PG Gross Checker
Dynamic	IR / AVG-EM / RMS-EM	<100%	Large drivers / Large arrays Decap check Jitter specific concerns
Signal-EM	AVG-EM / RMS-EM	100%	Mixed-Mode Signal-EM enables 100% coverage

Figure-3: Sign-off coverage requirements for FPGA designs

Input Data Requirements

The flow uses industry standard input data for the IPs including GDSII formatted layout information, Spice net-list in the DSPF/SPEF format, and test-bench or input vectors in the Spice format. If the analog or mixed signal design is an IC by itself, the package layout will be necessary for a full-chip level analysis. Other inputs necessary are the technology parameters through the iRCX format or other industry standard formats like the nxtgrd, device model data, and layer mapping information (necessary to translate the GDSII data).

Modeling and Simulation Flow for Power Noise Analysis

The usage flow for performing power noise analyses using the flow is illustrated in *Figure-4*. The flow uses Apache Design's Totem and RedHawk platform to achieve analysis and simulation environment. Once the required input data are available, the first step in the process is to perform the setup and the "pre-characterization" of the circuit. Then the layout and the pre characterization data are read in along with the optional package layout or net-list information to perform the necessary simulations (i.e. grid-check, DC and/or transient). Next, the weakness and hot-spot analysis can be done along with interactive design fixing to isolate and rectify the issues in the design. Subsequently a transistor level model can be written out for full-chip level analysis.

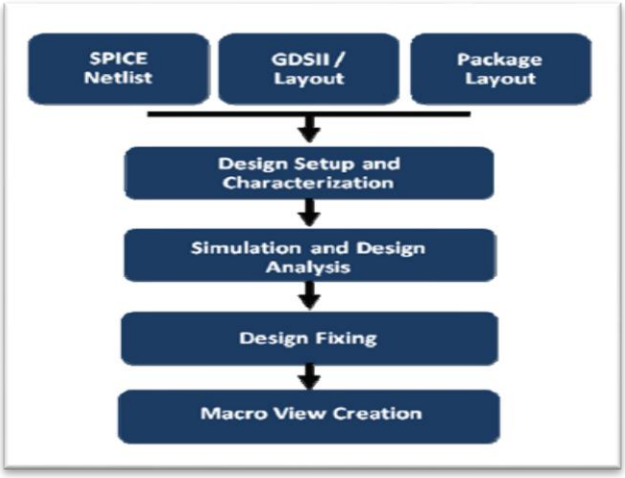

Figure-4: Static and Dynamic Voltage Drop Analysis Flow

The Dynamic voltage drop on the power-grid is defined by V(t) = i(t)R + Ldi/dt where i(t) is the total instantaneous current (sum of the transient switching current is(t) and the capacitor current ic(t)) and L represents the on-chip and package self and mutual inductances. *Figure 5* shows a schematic representation of two inverters in a chip, one of which is switching and one of which is not switching. In this circuit, the package and wires are represented as R, L and C elements. To perform a transient analysis and obtain a voltage and current information one would typically use Spice. However, given the complexity and size of today's chips and IPs, Spice simulators cannot perform this analysis within a reasonable time-frame and may lack the capacity.

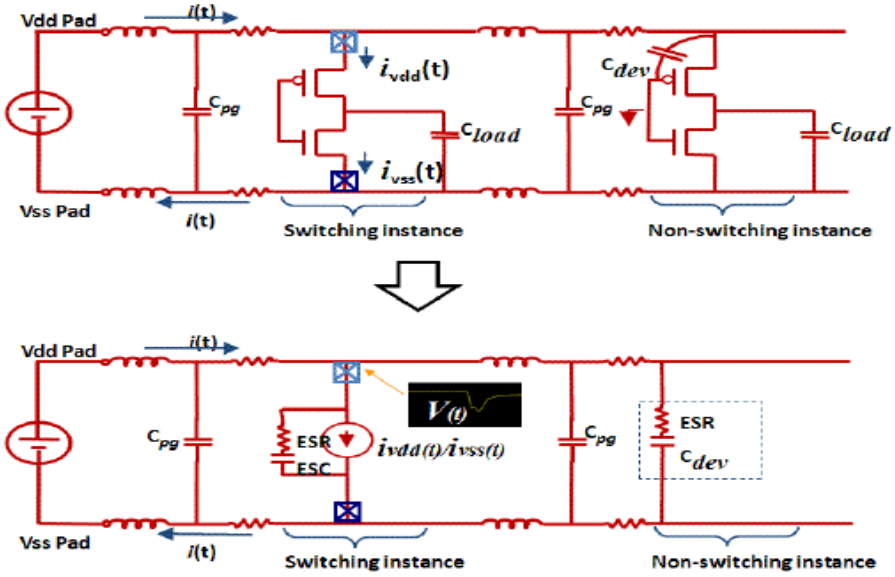

Figure-5: Circuit Modeling Details in the flow

The flow is able to perform analysis for large IPs and maintain the spice level accuracy through the use of several techniques. First it transforms the "non-linear" nature of the circuit into a "linear" form by pre-characterizing the current, intrinsic resistance, and device capacitances for each transistor in the circuit. Every transistor is replaced by its own such model.

The flow will then extract the power and ground network RLC elements, which along with the package/board (if relevant) parasitic is used to simulate for the power/ground noise in the circuit. The transistor models act as current sinks while the parasitic network provides the impedance. The capacitances in the circuit can come from various components like the PG mesh capacitance, device diffusion and gate capacitances, signal line capacitance, and intentional capacitances both on the die and in the package and board. By solving this "linear" circuit with its proprietary solver technology, the flow provides the current and voltage information at every wire, via, and transistor in the circuit. The first step in using the flow involves the "pre-characterization" of the circuit. This is done using the circuit Spice net-list, device models, and an input vector set. The circuit is then simulated with industry standard Spice solution. During this step, the

devices are supplied with a constant voltage at the power and ground terminals (i.e. without involving the power/ground network parasitic). Thus the capacity and run-time limitation seen in other solutions which attempt a combined analysis is not encountered here. However, the flow still delivers accuracy similar to such solutions by using several techniques which will be described in the following sections.

After the characterization is done, the flow reads in the design layout. Specifically the geometries of the power and ground network of the IP down to the contact/diffusion are required. A universal design format common to the design industry is the GDSII format. The flow reads in the design GDSII and creates a model of the power and ground geometries along with the location of transistors as shown in *Figure 6*. The entire flow, from the first step to the last, is a single pass flow done in an integrated manner. However for clarification and understanding, the intermediate steps are described in more detail below. The first stage in the simulation process, shown in *figure 7* is the extraction of the power and ground parasitic network. In this stage, the flow uses an integrated, high-performance RLC parameter extraction engine to obtain the parasitic of the PG network.

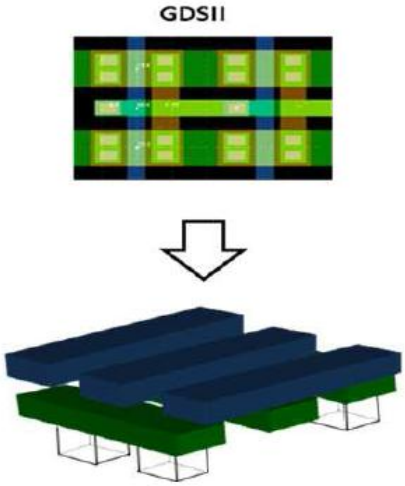

Figure-6: GDS Modeling

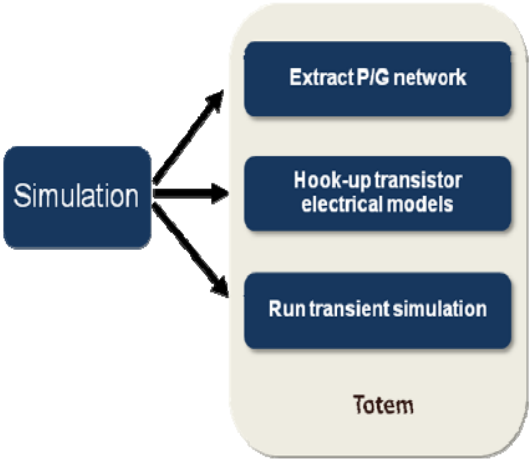

Figure-7: Simulation Flow

The extraction engine technology which leverages the regularity in on-die power / ground mesh networks to provide the run-time and capacity needed to simulate the largest of designs. The extraction is done on all the power domains in the design and can selectively include the capacitance and inductance of the mesh as needed (for example, static/DC analysis does not require a C and L extraction of the P/G mesh).

Every transistor is replaced with its equivalent, pre-characterized model. For static/DC analysis, an average or the peak of the device current can be used in the current sink. For the transient/DvD analysis, the true characterized transient current profile is used along with the associated effective transistor resistance and capacitances. For static analysis, the DC voltage and current is computed for every wire and via starting from the voltage

sources to the transistors. For the transient analysis, time-domain current and voltage waveforms are calculated for each wire and via. The flow DvD analysis modulates the transistor current based on the voltage seen at that transistor. This is possible since the pre-characterization of the transistor current to generate the APL was done for multiple voltage levels. This adaptive de-ration of the current drawn by every transistor at every simulation time-step based on its supply voltage enables the flow to deliver Spice accurate results at a full IP or even at the full-chip level. The default time-step for the transient analysis in the flow is 10ps.

BLOCK TYPE	ANALYSIS	BLOCK DYNAMIC	
		Vectored	Vectorless
Custom	Power EM/IR	Transistor Level Vectored	
	Signal EM	Transistor Level Analog → Vectored/Mix-Mode Digital → Vectorless	
P&R	Power EM/IR	Cell Level Vectorless	
	Signal EM	Cell Level Vectorless	

Figure 8: Design Styles and Required Analysis

The electro-migration for the wires and vias are simultaneously determined based on the currents flowing through the different nodes of the power and ground mesh. For static analysis, DC or average EM limits are checked. For transient, average, RMS, and peak EM limits are checked for possible violations. The RMS and peak EM checking is possible since the flow does a "true" time-domain analysis to get a waveform of the current flowing in every wire and via in the circuit. The flow supports all the advanced EM limits and rules. Additionally it provides the designers with access to the data-base to obtain current flow and associated routing topology information for every wire and via. This information is particularly needed if the designers want to write their own EM rules.

Signal Line Reliability Analysis Flow

The flow provides a single platform approach to analyze power line and signal interconnect EM in a design. Power EM analysis is performed as part of static and/or dynamic analysis. Signal EM analysis, which is performed in a separate run, checks for average, RMS, and peak current densities in all signal wires and vias. The signal EM analysis provides text-based reports and graphical maps for reporting and debugging. Both vector-less and vector based approach are available in the flow. Vector-less provides acceptable accuracy in the flow and detailed coverage which can be missed with the vector based approach especially for the signal EM reliability analysis. How to

choose which block goes through which sign-off approach, the following methodology shown in *Figure-8* is used.

Signal EM capability uses a similar approach to the power EM modeling flow in which the switching currents for transistors connected to signal nets are pre-characterized and used to model the RMS, average and peak currents on a signal net. Once the currents are captured, the value is compared against the specific current limits specified in the technology file. The EM limits can be specified in the technology file as a dependent on physical parameters including the width of the wire, length of the wire, size of the via, and temperature of the die. The EM limits can also be specified as a polynomial dependent on width or length to support advance process nodes. The flow details are shown in *Figure-9.*

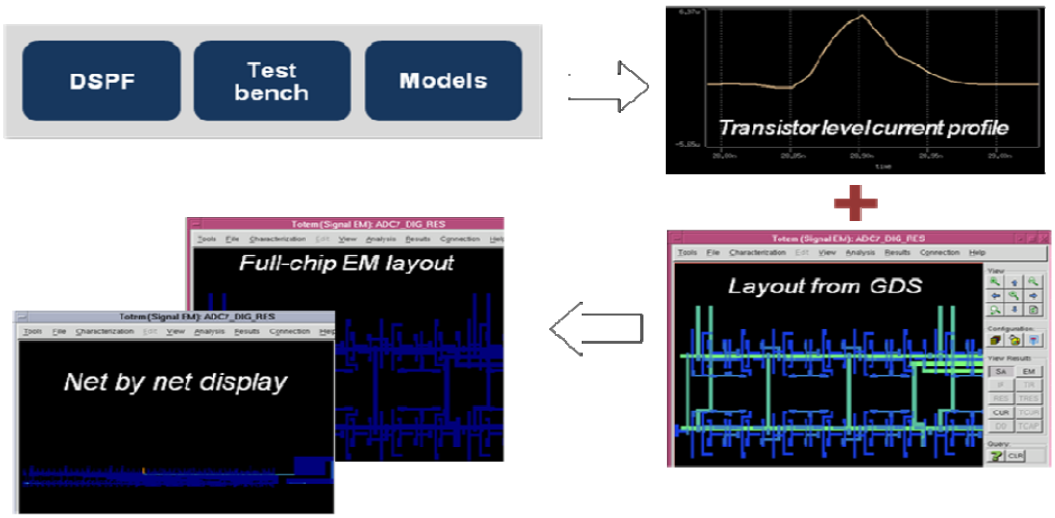

Figure 9: Signal EM Analysis flow with vectored approach

Vector-less Signal EM Methodology:

Vector-less signal EM methodology is used to achieve 100% coverage across the designs and be able to signoff electro migration on each signal net in the design, meeting the foundry requirements. The flow works of basic inputs , which are used to construct a current waveform at the driver output and the transient analysis capability solves for the AVG/RMS/PEAK current across each wire/via segment on the signal net under analysis.
Figure-10 describes an example on how the current waveform is constructed using various parameters provided for a net under analysis.
User need to provide net properties as follows:

- Output Slew
- Frequency of the net
- Toggle Activity
- Load and Resistance is extracted by the tool

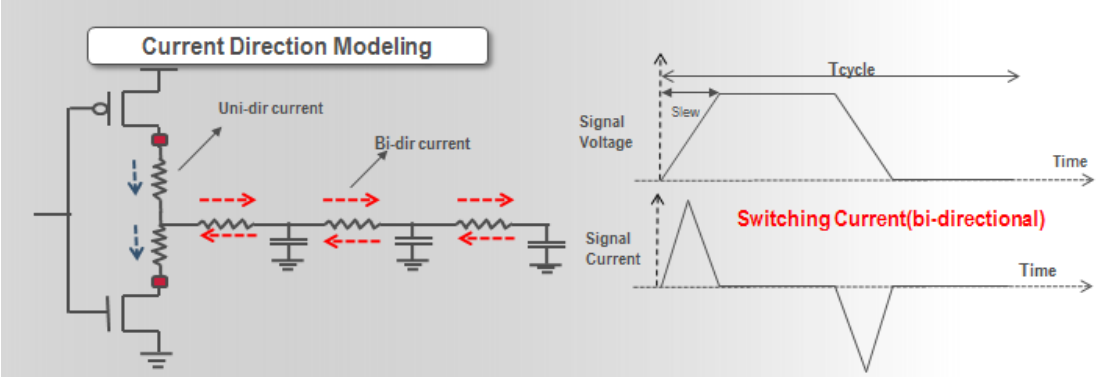

Figure 10: Example of current waveform construction in v-less flow

Full-Chip Signoff Methodology:

The design methodology employed in today's FPGA chips is a bottom-up approach. The IPs are designed and validated independently by one team and the full-chip is integrated by a separate team. (*Figure 11* shows a high level overview of an FPGA design). This methodology promotes design and IP reuse and also accelerates the FPGA integration process. However, this flow imposes certain challenges on the power noise verification methodology as it needs to fit in with the "bottom-up" design methodology. It requires the capabilities to perform block/IP level analysis with the flexibility to model top level connectivity and noise coupling scenarios.

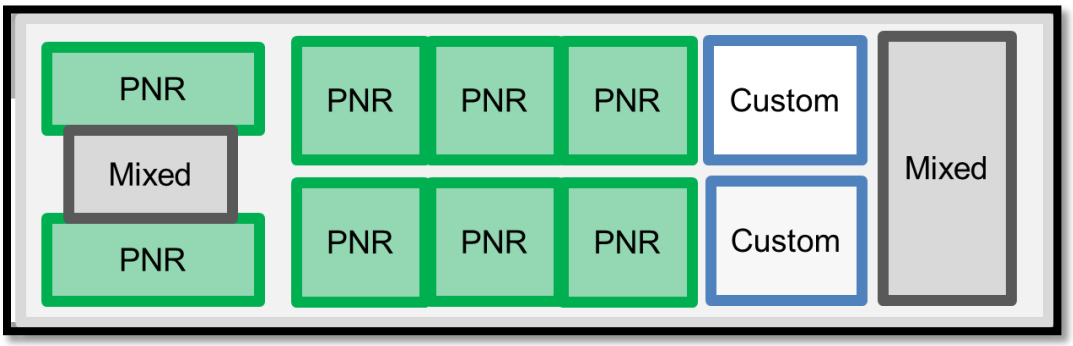

Figure 11: High Level View of a 20nm Full-Chip FPGA

Once the block or IP has been validated, this solution should enable model creation with the possibility to embed IP level design constraints like maximum allowed voltage droop, etc. This model should provide transistor level detail but allow full-chip level analyses without compromising run-time and capacity needs. At the full-chip level, the power noise analysis solution should consider the models of one or more IPs along with other

logic and perform a global power noise simulation incorporating the package and board effects.

The full-chip analysis must provide feedback to the IP designers about the impact of noise source on their blocks from the switching in a full-chip context, be it through the shared power-ground mesh, or the coupling from high energy in specific frequency bands of interest.

The CMM models can be used for full-chip analysis of mixed signal design without compromising accuracy and runtime. The flow can simultaneously simulate the switching behavior of standard cells and the analog and custom blocks using their respective CMM model in the same run. This helps designers to verify the top level connections to the CMM blocks under various coupling scenarios in mixed-signal blocks. It also helps assess the impact from the switching of mixed-signal blocks on the shared or coupled power and ground networks.

Mixed-signal designs are typically divided into two categories, namely, Large Digital/Small Analog and Large Analog/Small Digital designs. The flow can seamlessly model and simulate these two types of designs based on the LEF/DEF of digital blocks and the CMM physical models of the analog circuits.

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