DesignCon® 2014

Touchstone®v2.0 SI/PI S-Parameter Models for Simultaneous Switching Noise (SSN) Analysis of DDR4 Memory Interface Applications.

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UBM Tech

Agenda

- Introduction
- Touchstone®v2.0 file format
- Power aware IBIS v5.0 IO models
- DDR4 Simultaneous Switching Noise Analysis
- System Level Design Considerations
- Summary and Conclusion

Introduction

- Simultaneous Switching Noise (SSN) is a concern for high speed parallel memory interfaces such as DDR4 due to high data rates
- Accurate SSN Analysis requires both SI/PI S-parameter models for the package and channel as well as power aware IBIS v5.0 models for drivers and receivers
- DDR4 architectural design considerations
- SSN simulations should be performed using a highly accurate transient-convolution simulation engine for high port counts

Touchstone®v2.0 Overview

- Touchstone®v2.0 offers several accuracy improvements relative to Touchstone®v1.0 format
- Per port reference impedances is one of the key accuracy improvements which allows one to have data and address nets as well as power and ground nets in the same file with better accuracy than using v1.0 file format
- Normalize power nets to 100mOhm and signal nets to 50 ohms within same S-parameter model file

Touchstone® v2.0 Syntax

- The following is an example of a simple 4-port Version 2.0 header and option line:

[Version] 2.0

 # GHz S MA R 50

[Number of Ports] 4

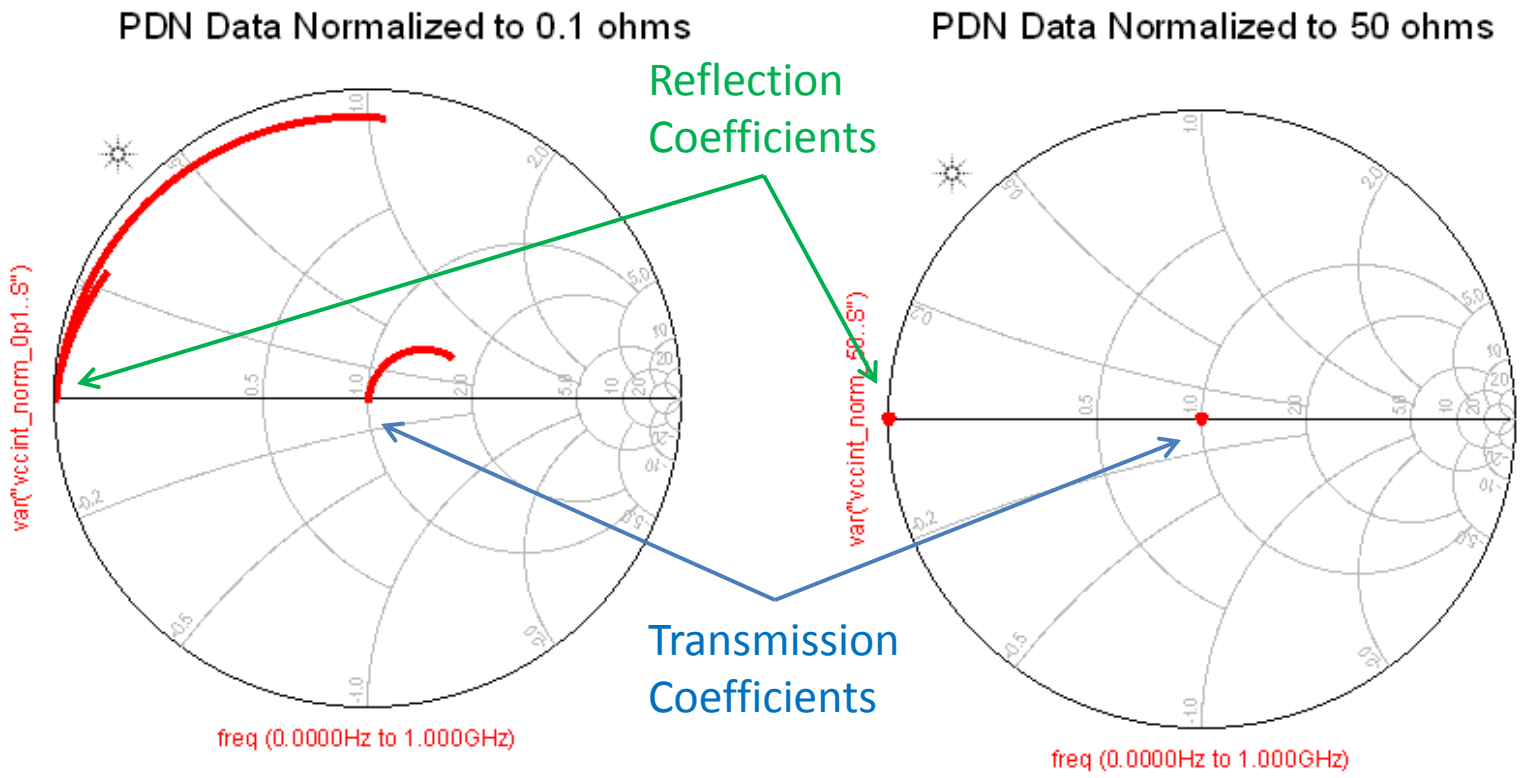
[Reference]

50 50 0.01 0.01

[Number of Frequencies] 50

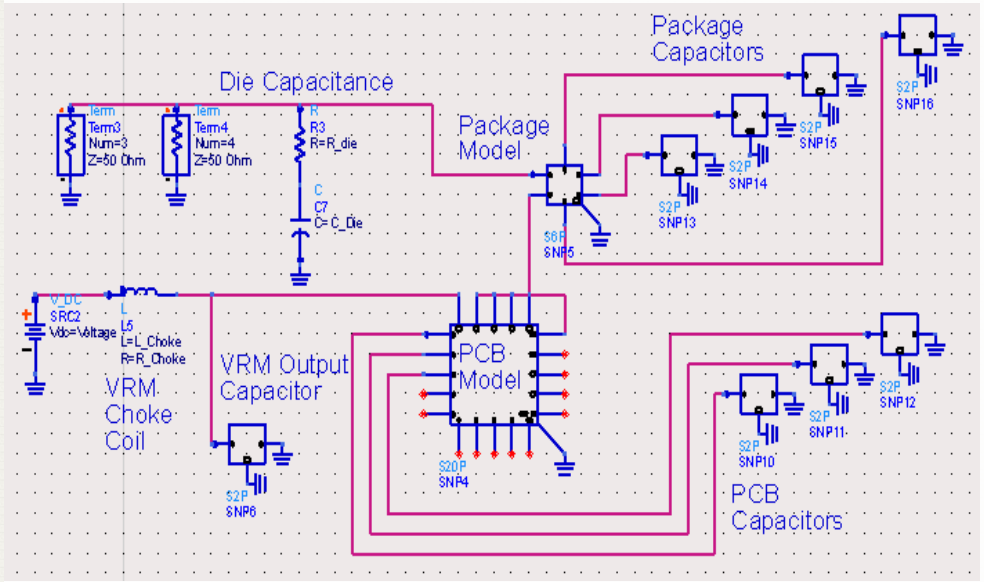
Per Port Reference Impedances

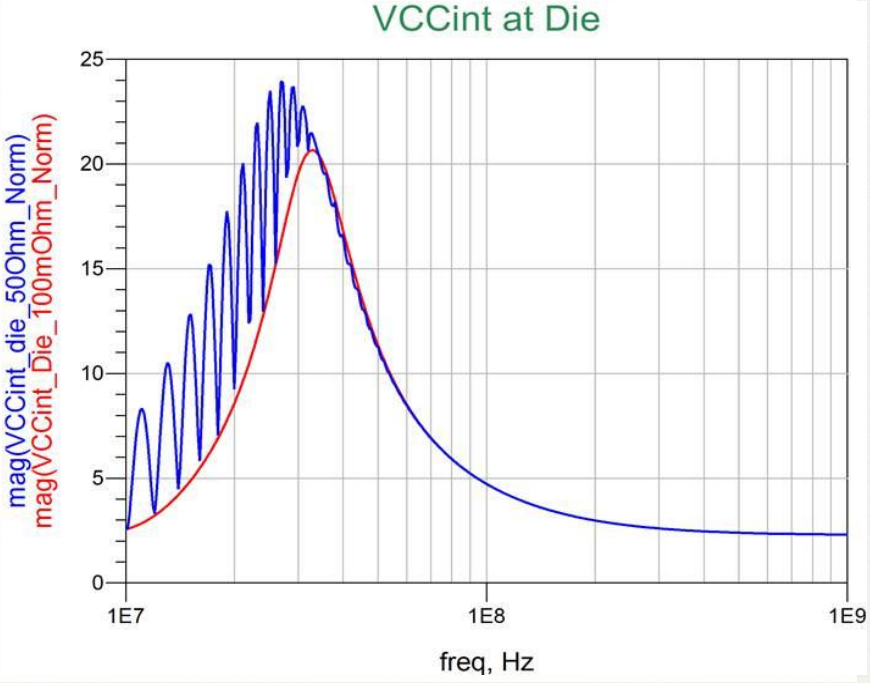
- The data normalized to 50 ohms is compressed around the origin (center of chart) and along the left edge of the chart. The data normalized to 0.1 ohms is well spread out on the Smith Chart



Simulation Convergence is Related to Reference Impedance

- Data normalized to 0.1 ohms (plotted in red) using v2.0
- Data normalized to 50 ohms (plotted in blue) using v1.0
- Non-convergence of the simulation results when using 50 ohm data as compared to the smooth shape of the 0.1 ohm data

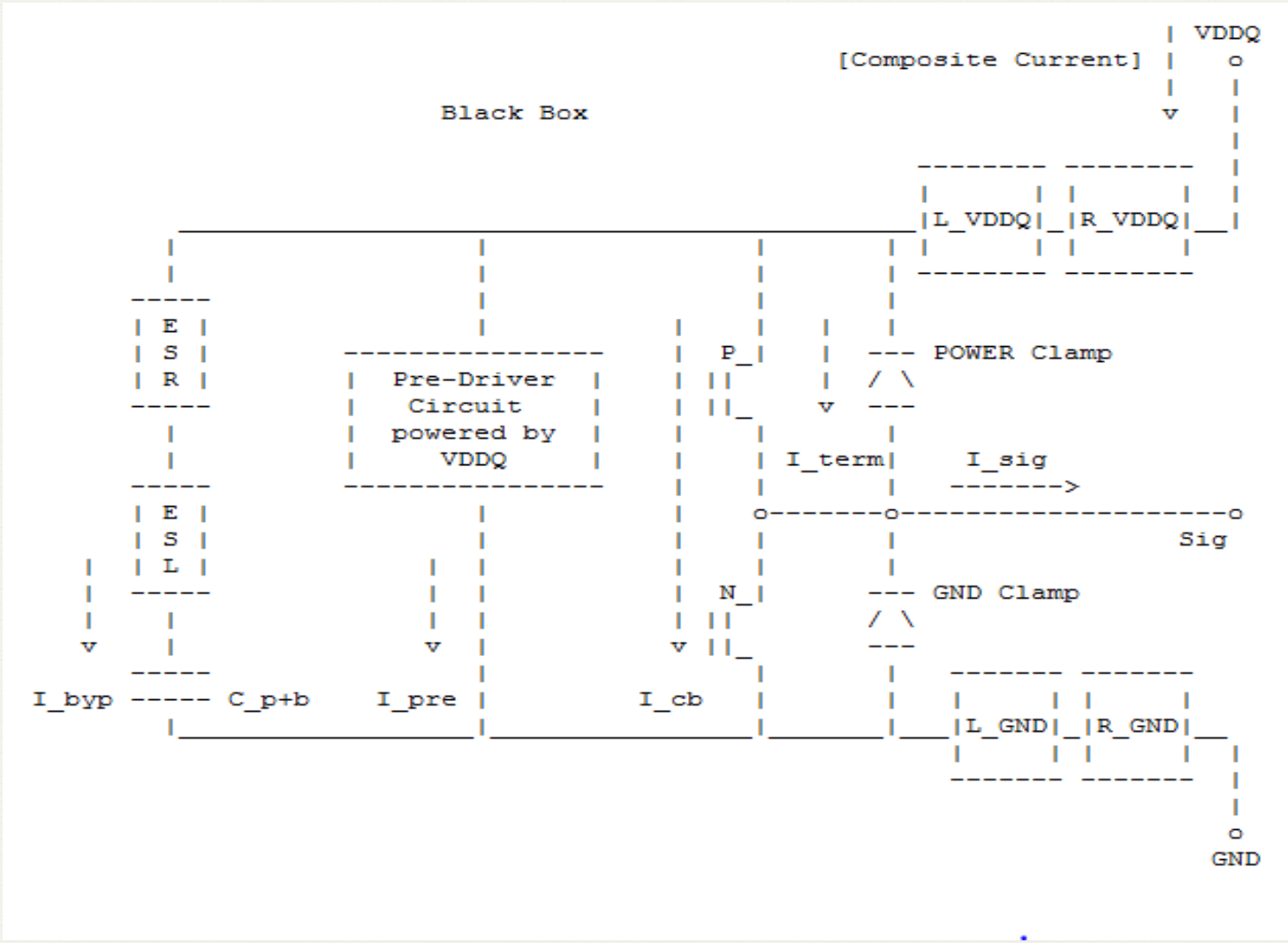




IBIS v5.0 BIRDs for SSN Simulations

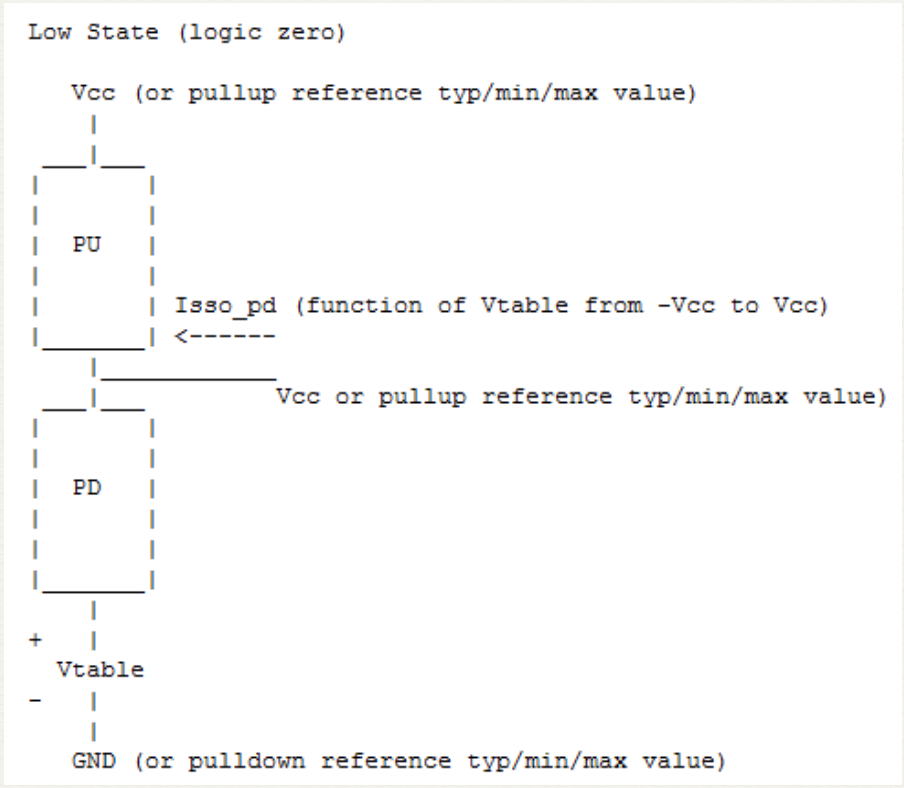
- BIRD 95.6 Power Integrity Analysis using IBIS
  - Keyword [Composite Current]
  - Models VCC currents under specific loading conditions
- BIRD 98.3 Gate Modulation Effect (table format)
  - Keywords [ISSO PU] and [ISSO PD]
  - Models output impedance variation as a function of VCC voltage
- BIRD 76.1 (v4.0) Additional Information Related to C_comp Refinements
  - Keywords [C_comp_pullup] and [C_comp_pulldown]
  - Models as IO pad capacitance to VCC and GND separately

BIRD 95.6 Power Integrity Analysis using IBIS

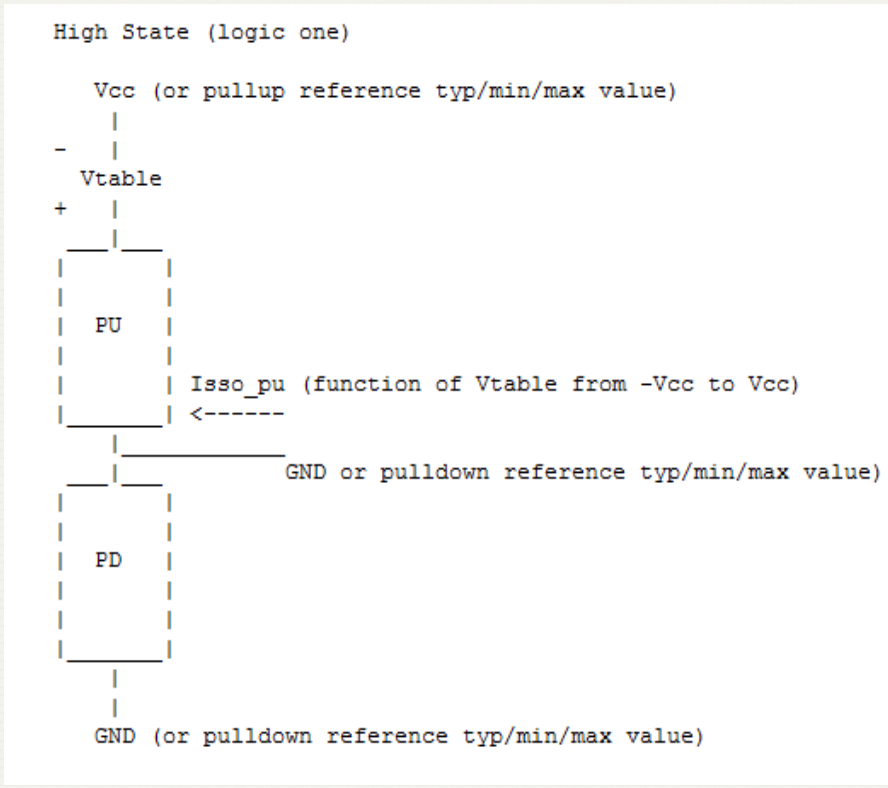


BIRD 98.3 Gate Modulation Effect

ISSO PD

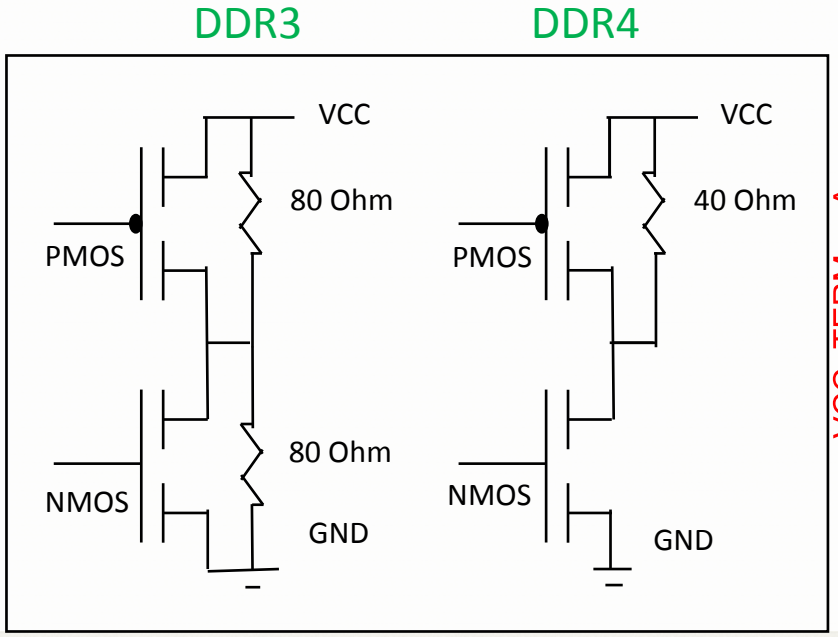


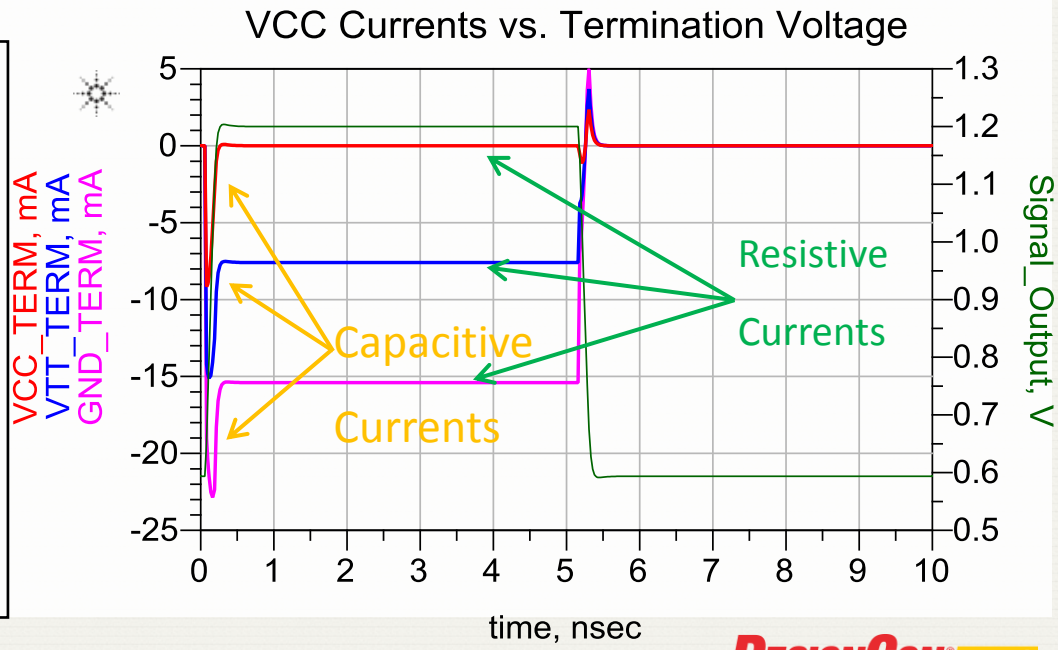
ISSO PU



Power Distribution Network Noise and Termination Voltage

- DDR4 uses POD12 (Pseudo-Open Drain Logic) with VCC termination while DDR3 uses SSTL (Short Stub Transceiver Logic) with VTT termination
- DDR4 has a data bus inversion feature which ensures that a maximum of half of the data bus signals will switch on each clock edge which significantly helps reduce SSN



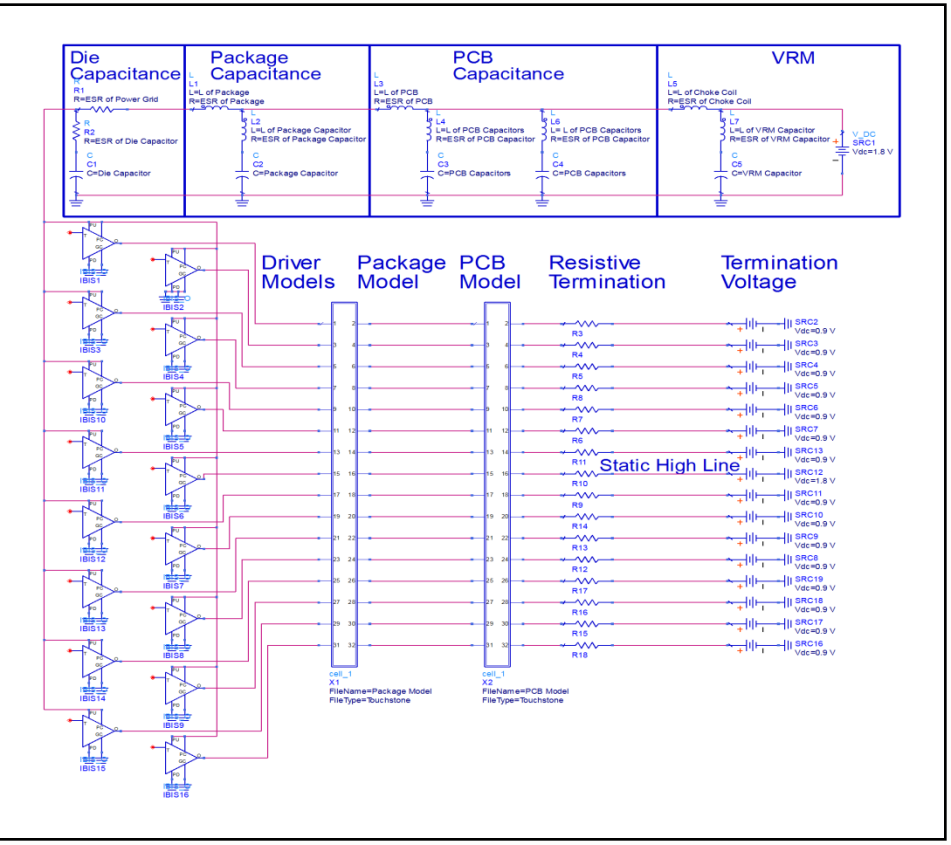


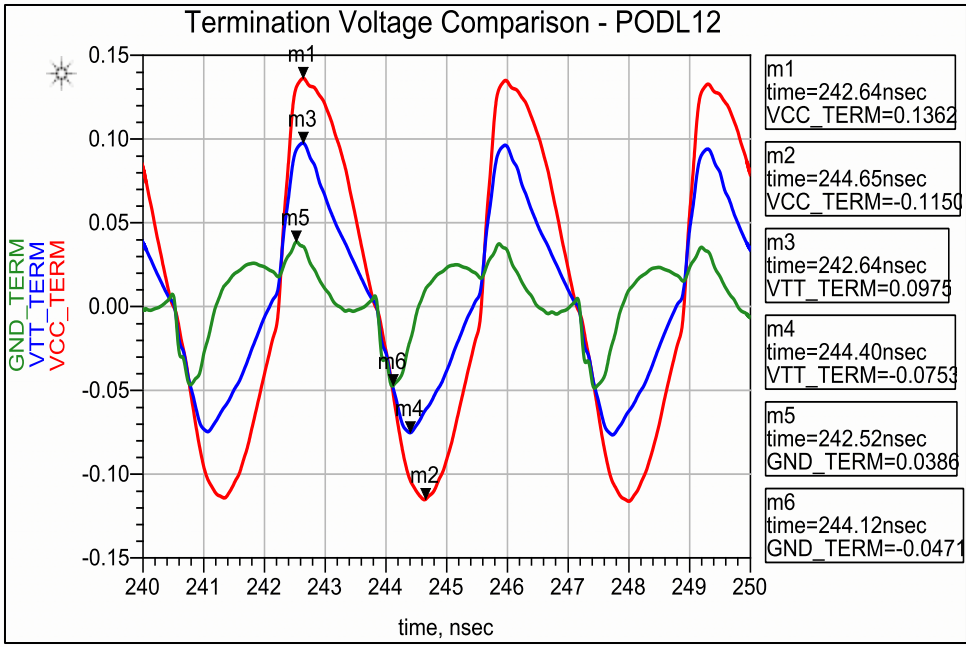
DDR4 SSN Simulation

- Agilent Advanced Design System 2013.06 was used to perform the DDR4 SSN simulations used in this presentation.
- ADS has the capability to bring together the 3 necessary elements
  1. Support power-aware IBIS v5.0 models for memory controller and DDR4 memory devices
  2. Support Touchstone v2.0 SI/PI S-parameter package and channel models
  3. Accurate causal responses using transient-convolution simulation engine for large port count (n>100) SI/PI S-parameter models.

DDR4 POD12 vs. DDR3 SSTL15 Power Supply Noise

- Changing the termination voltage from DDR3's VTT to DDR4's VCC results in much lower power supply noise

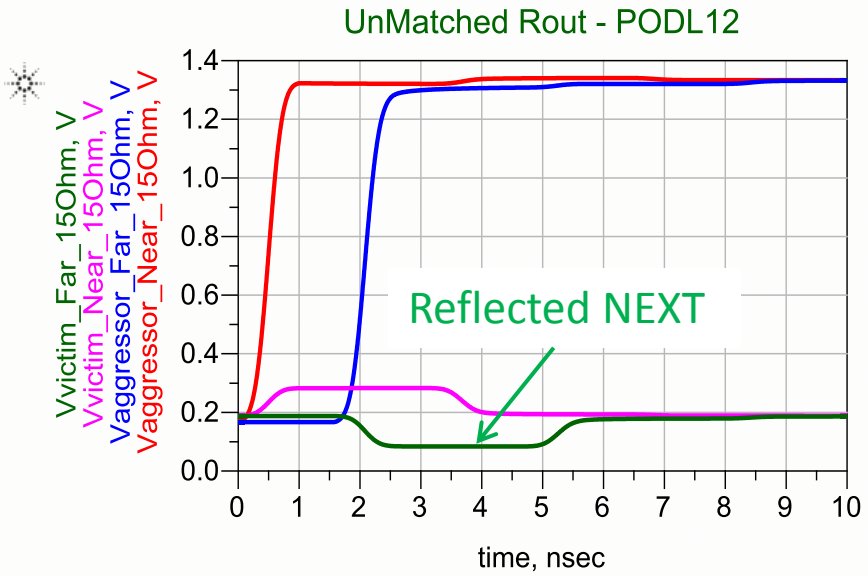


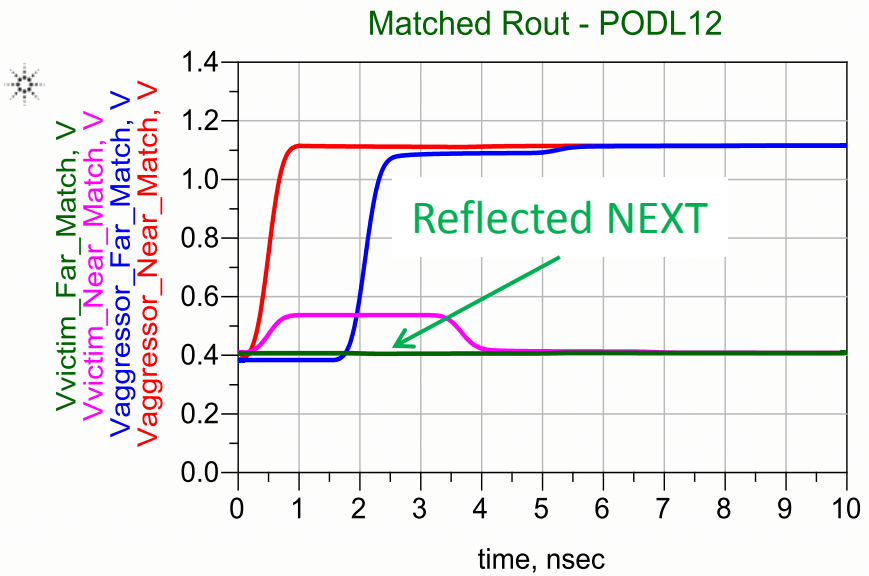


IO Standard	Termination (Volts)	Termination (Ohms)	Minimum (mV)	Maximum (mV)
PODL12	VCC=1.5	40	-47	39
PODL12	VTT=0.75	40	-75	98
PODL12	GND=0	40	-115	136

DDR4 Memory Controller - Crosstalk Reduction

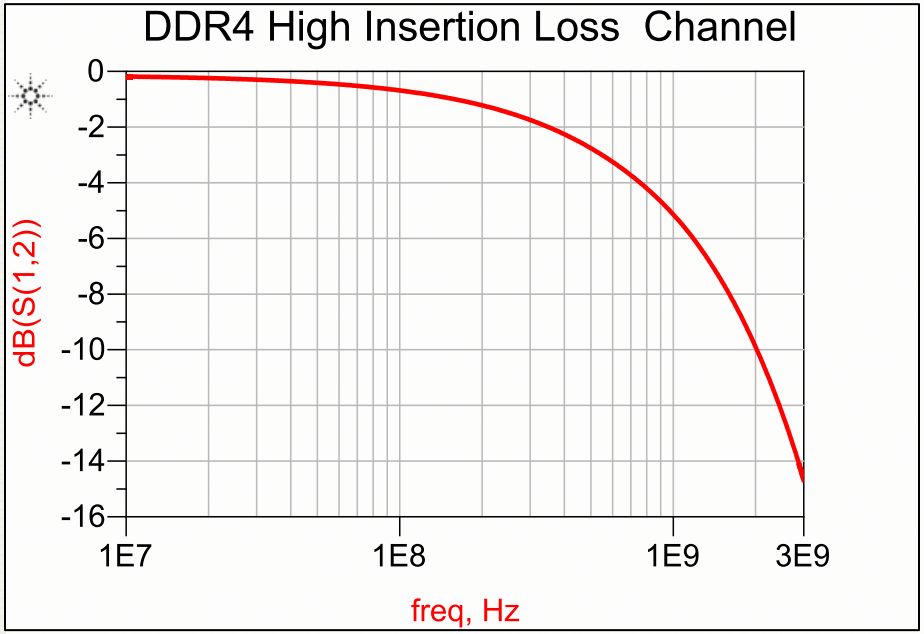
- In PCB Stripline transmission lines, crosstalk is mostly associated with reflected NEXT (Near End Crosstalk)
- Matched output impedance of drivers can minimize crosstalk

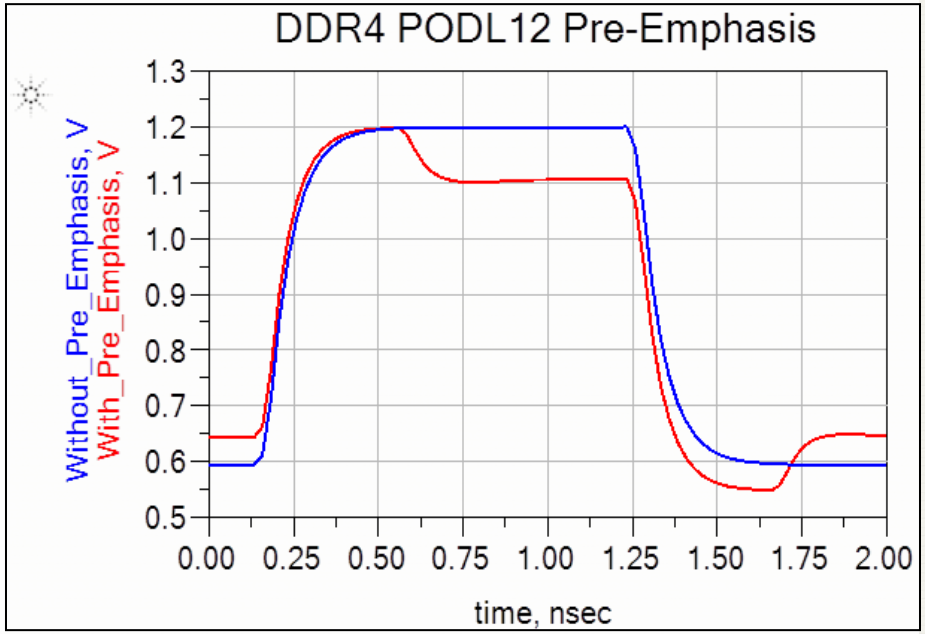




DDR4 Memory Controller Pre-Emphasis

- To compensate for the channel's high insertion loss, the memory controller's driver architecture may require pre-emphasis.
- Example insertion loss shown using standard FR-4 PCB material

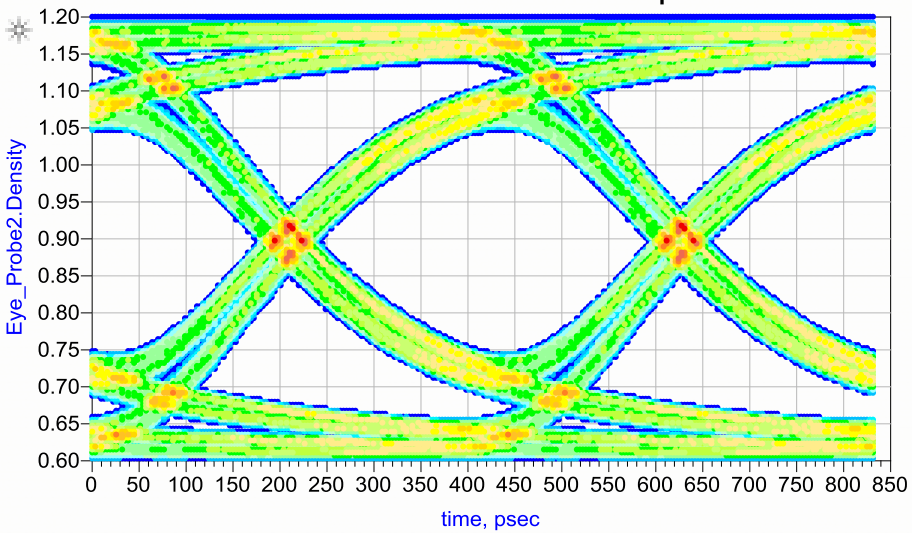




Memory Controller 2 dB Tx Pre-emphasis

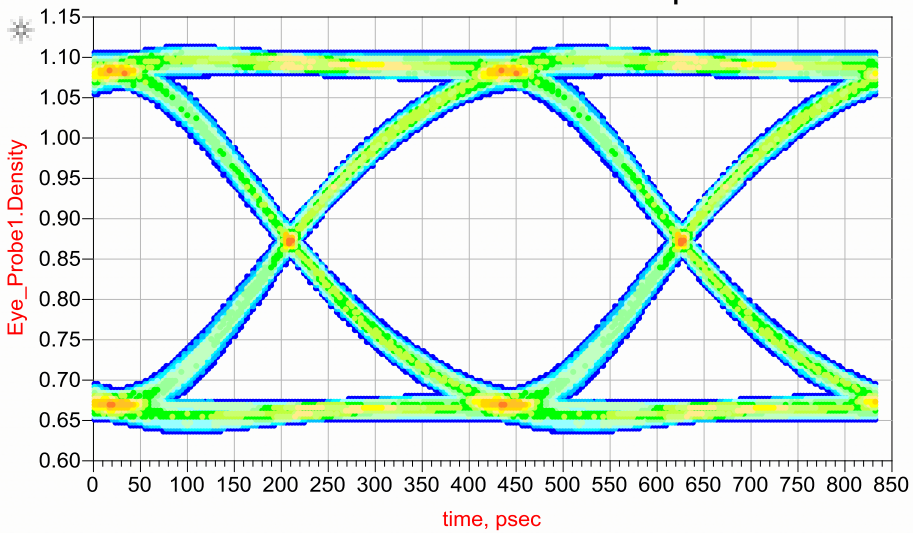
- Using 2dB of pre-emphasis increases eye width by 38pS (from 354pS to 392pS) and eye height by 69mV (from 259mV to 328mV)
- PRBS15 pattern at 2400 Mbps data rate

PODL12 - Without Pre-Emphasis



measurement	Eye_Probe2.Summary
Level1	1.120
Level0	0.677
Height	0.259
Width	3.542E-10

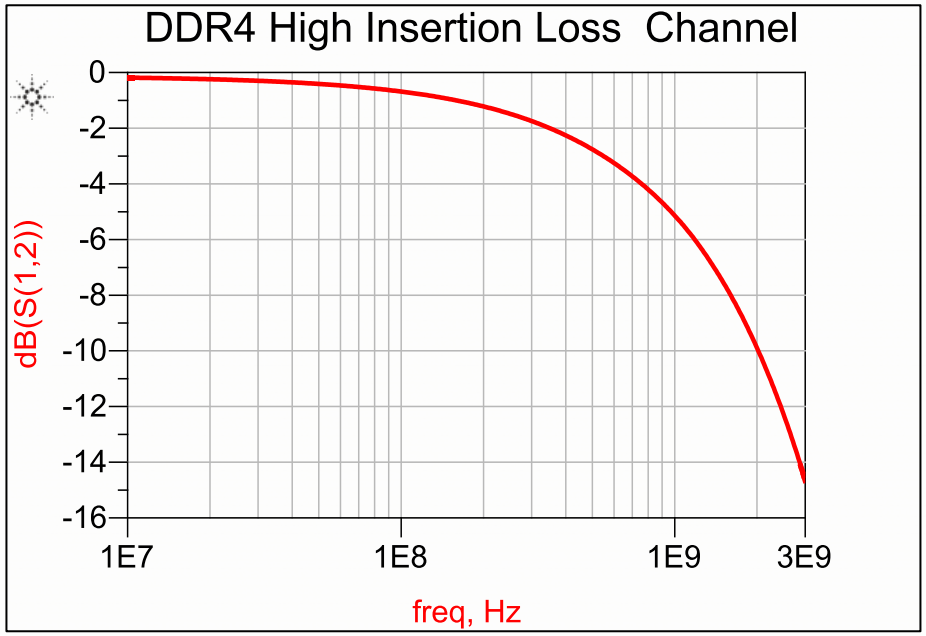
PODL12 - With 2dB Pre-Emphasis

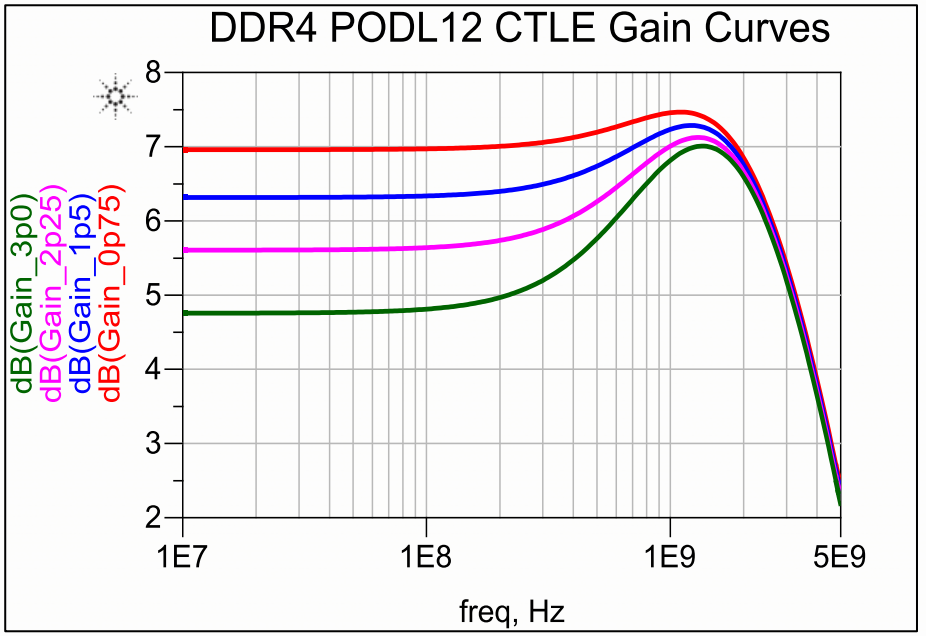


measurement	Eye_Probe1.Summary
Level1	1.079
Level0	0.673
Height	0.328
Width	3.917E-10

DDR4 Memory Controller - CTLE

- To compensate for the channel's high insertion loss, the memory controller's receiver architecture may require CTLE.
- Example insertion loss shown using standard FR-4 PCB material

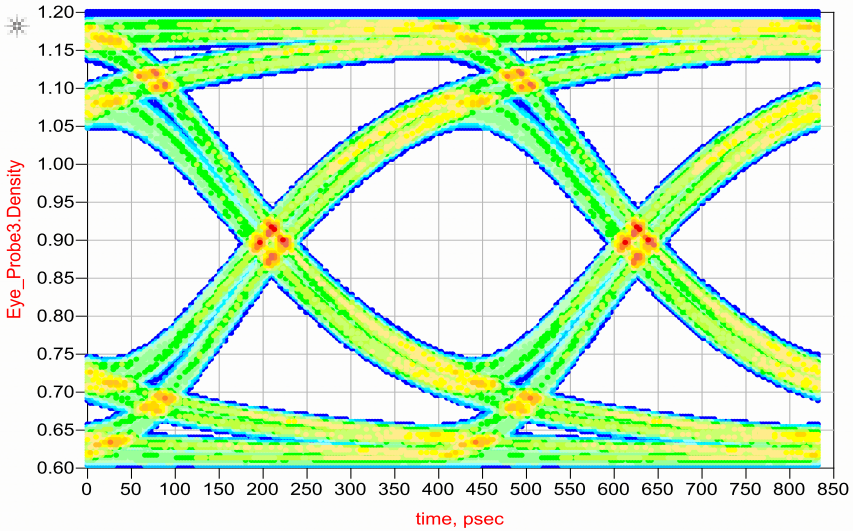




DDR4 Memory Controller Rx CTLE with 3dB Gain

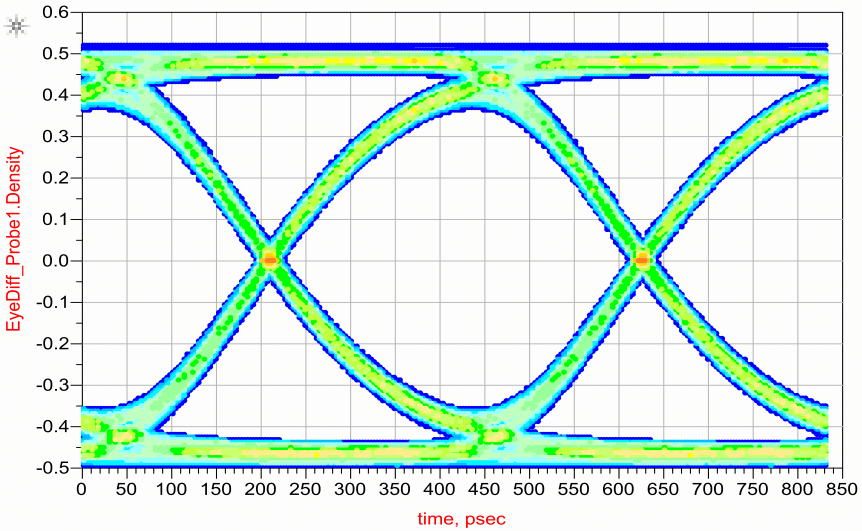
- Using 3dB of CTLE increases eye width by 36pS (from 354pS to 390pS) and eye height by 64mV (from 259mV to 323mV)
- PRBS15 pattern at 2400 Mbps data rate

Without CTLE



measurement	Eye_Probe3.Summary
Level1	1.120
Level0	0.677
Height	0.259
Width	3.542E-10

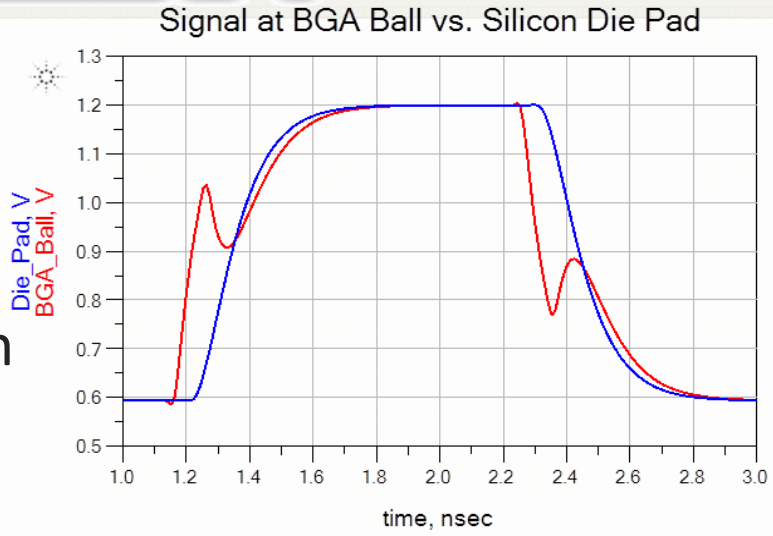
With 3dB of CTLE

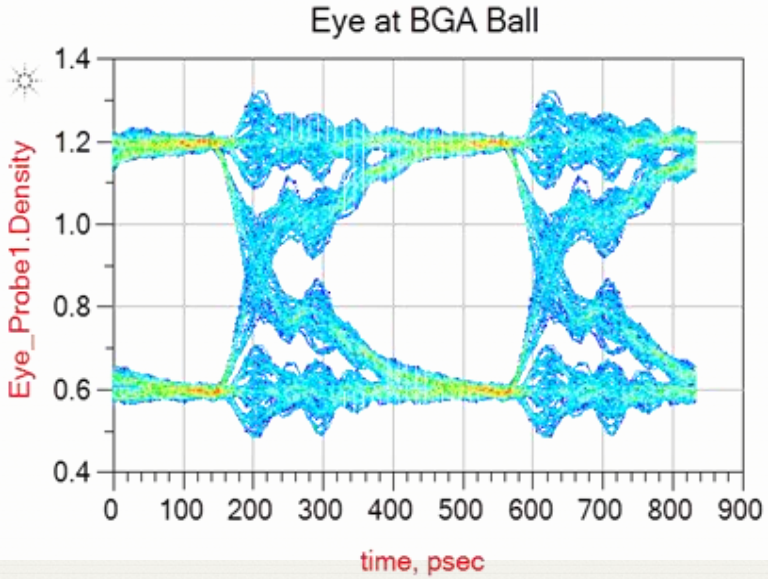


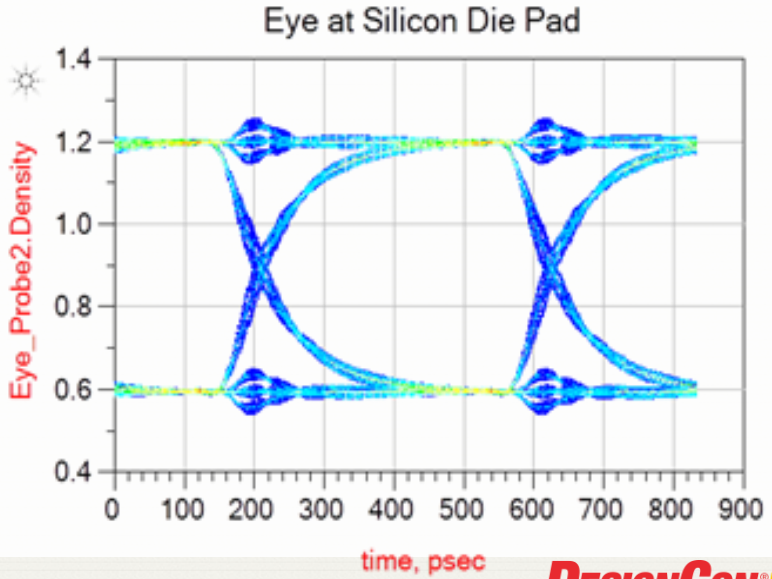
measurement	EyeDiff_Probe1.Summary
Level1	0.437
Level0	-0.421
Height	0.646
Width	3.896E-10

Eye Diagram at Different Physical Locations

- Due to the silicon die capacitive loading and the (package + PCB stub) electrical delay, a reflection may appear in the transition region of both rising and falling edges







Measuring at the Different Physical Locations

- During lab measurements the additional channel between desired probe point and actual probe point can be de-embedded.
- For the de-embedding one has to provide the touchstone file of the extra channel which is normally obtained via simulation techniques.
- Another technique that can be used during measurement (on the DRAM side) is to use a DDR4 BGA interposer. The accessibility of all the probe points improves dramatically with the interposer and the extra channel offered by the interposer is automatically de-embedded

Conclusion

- To Simulate SSN for DDR4 memory applications requires the following three key elements:
  1. Touchstone ®v2.0 SI//PI package and channel S-parameters models
  2. Power aware IBISv5.0 models for drivers and receivers
  3. High accuracy transient-convolution simulation engine for high port counts
- To achieve high data rates for DDR4 memory applications, the memory controller may require the following key architectural features:
  1. Highly linear matched output impedance driver
  2. Tx Pre-Emphasis
  3. Rx Continuous Time Linear Equalizer (CTLE)