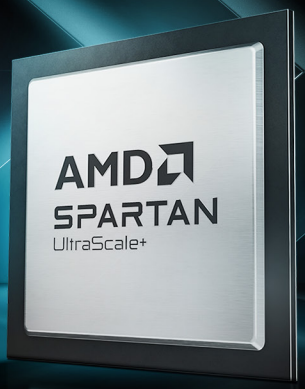
AMD SPARTAN ULTRASCALE+ FPGA

The AMD cost-optimized, high I/O Spartan UltraScale+ family built for secure, low-power applications



OVERVIEW

The AMD Spartan™ UltraScale+™ FPGA family is optimized for cost-sensitive applications requiring high I/O count, low power, and state-of-the-art security features. With densities ranging from 11K to 218K logic cells and up to 572 I/Os, Spartan UltraScale+ FPGAs excel in a wide range of use cases, from I/O expansion and board management to sensor processing and control.

Built on the UltraScale™ architecture, the 16 nm Spartan UltraScale+ family complements AMD's other FPGA cost-optimized devices including Artix™ UltraScale+, Artix 7, Spartan 7, and Spartan 6 FPGAs.

Supported by AMD Vivado™ design tools, Spartan UltraScale+ FPGAs offer a proven solution for your next project.

HIGHLIGHTS

HIGH I/O, LOW-POWER FPGAS WITH STATE-OF-THE-ART SECURITY FEATURES

- Highest I/O to logic cell ratio[1] in the AMD Cost-Optimized Portfolio (COP)
- Interface flexibility with 1.2V to 3.3V I/O, 16.3 Gb/s transceivers
- Simplified connectivity PCIe® Gen4, MIPI D-PHY, and LPDDR4x/5
- Up to 30% power reduction[2] with 16nm FinFET & power efficiency through hardened DDR and PCIe®
- Advanced security features to protect your IP, prevent tampering, and maximize uptime

GET TO MARKET FAST WITH PROVEN VIVADO TOOLS

- Maximize development efficiency with end-to-end IDE spanning synthesis, place and route, simulation, and debug
- Minimize onboarding with single IDE for broad portfolio: 28 nm, 20 nm, 16 nm, and 7 nm

DESIGN ONCE WITH A TRUSTED SUPPLIER

- Nearly four decades of industry experience
- Support 15+ years of product lifecycle
- Worldwide Distribution, Sales, and Support

KEY APPLICATIONS

INDUSTRIAL AND EDGE:

Factory Automation and Robotics

IIoT Gateways and Edge Appliances

Smart City and Smart Grid

HEALTHCARE AND SCIENCES:

Medical Equipment

Imaging (Ultrasound, CT/MRI, Endoscopy)

WIRED AND WIRELESS:

Wireless Infrastructure

Access Network and Connectivity

DATA CENTER AND CLOUD:

Storage Acceleration

Data Center Interconnect

FEATURES

FEATURE	HIGHLIGHTS
High I/O Count	• High I/O count across portfolio – 304 to 572 GPIO • Three GPIO types to cover a wide range of requirements: High Density I/O (HDIO) up to 3.3V, High-Performance I/O (HPIO) up to 1.8V, and XP5IO up to 1.5V, supporting 3200 Mb/s MIPI and 1800 Mb/s LVDS
MIPI Support	• Up to 3200 Mb/s supporting advanced vision sensors (MIPI, SLVS-EC) • Up to 4-lane MIPI channels supported
High-Performance Transceivers	• GTH transceivers supporting up to 16.3 Gb/s • Single oscillator for fabric and SerDes eliminates extra clocking components
PCI Express® Gen4 Support	• PCI Express Gen4 x8 support • DMA IP further simplifies interfacing
Versatile Memory	• On-Chip Memory: Block RAM for low latency, high throughput, and UltraRAM provides massive on-chip memory • External Memory: LPDDR4x and LPDDR5 via hardened memory controllers up to 4266 Mb/s, and DDR4 soft memory controller IP up to 2400 Mb/s
Integrated Hard IP	• PCIe Gen4 x8 • LPDDR4x/5 Memory Controller • Platform Management Controller
State-of-the-Art Security Features	• Offers the most security features[3] of any AMD cost-optimized FPGA product • PQC with NIST-approved algorithms and AES-GCM for secure configuration • Each device is unique and identifiable through Physical Unclonable Function
Enhanced Programmable Logic Architecture	• Based on proven TSMC's 16 nm FinFET+ process • Voltage scaling to tune power and performance on the same device • Enhanced CLB/LUTs, routing, and ASIC-class clocking for high utilization

Scalability across the FPGA Cost-Optimize Portfolio enables design reuse from project to project.

	AMD SPARTAN UltraScale+	AMD ARTIX UltraScale+	AMD SPARTAN 7	AMD ARTIX 7
System Logic Cells	Up to 218K	Up to 308K	Up to 102K	Up to 215K
I/O Count	Up to 575	Up to 304	Up to 400	Up to 500
Transceivers	Up to 16.3 Gb/s	Up to 16.3 Gb/s	N/A	Up to 6.6 Gb/s

NEXT STEPS

Spartan UltraScale+ FPGAs are supported by comprehensive development tools, reference designs, IP catalog, and evaluation platforms.
For more information, visit **www.amd.com/spartan-ultrascale-plus**
To contact your local AMD sales representative, visit **www.amd.com/en/forms/product-inquiry/adaptive-socs-and-fpgas.html**

ENDNOTES

1. Based on AMD internal analysis December 2023, comparing the total I/O to logic cell ratios in the AMD product datasheets for Spartan™ UltraScale+™ FPGAs to previous generations of AMD cost-optimized FPGAs. (SUS-001)
2. Projection is based on AMD Labs internal analysis in January 2024, using Total Power calculation (Static plus Dynamic power) based on the difference in logic cell count of an AMD Artix UltraScale+ AU7P FPGA, to estimate the power of a 16nm AMD Spartan™ UltraScale+™ SU35P FPGA versus a 28nm AMD Artix 7 7A35T FPGA, using Xilinx Power Estimator (XPE) tool version 2023.1.2. Actual Total power will vary when final products are released in market, based on configuration, usage, and other factors. (SUS-003)
3. Based on AMD internal analysis in December 2023, using the product datasheets to compare the number of security features a in Spartan™ UltraScale+™ FPGAs to previous generation AMD cost-optimized FPGAs. (SUS-002)

DISCLAIMERS

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